ANALYSIS OF ZERO-CURRENT SWITCHING TOPOLOGIES AND STRATEGIES FOR THE POWER ELECTRONIC BUILDING BLOCK

Final Technical Report

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for

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14. ABSTRACT A zero-current switching (ZCS) topology that provides zero-current turn-off but full-load turn-on of the main swtiches is analyzed for switching losses. State-space models of a non-punch through insulated gate bipolar transistor and a power p-i-n diode are used to simulate the circuit response. The switching energy is compared to that for hard switching and for an auxiliary resonant commutated pole. A more general analysis of other ZCS circuit topologies and switching strategies is included in an appendix.

15. SUBJECT TERMS Zero-current switching, ZCS, Auxiliary Resonant Commutated Pole, ARCP, switching energy, state-plane.

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OBJECTIVE

The objective of this project was to investigate the performance of insulated gate minority carry devices such as the Insulated Gate Bipolar Transistor (IGBT) and/or MOS-Controlled Thryistor (MCT) in a zero-current switching (ZCS) topology. The particular topology of interest was the resonant bridge in which the main devices are turned-off under zero-current conditions. This circuit topology/switching strategy had been identified as promising ZCS topology/strategy in a previous study[1].

[1] A report from the previous study, updated slightly to improve clarity, is included in Appendix B. This study represented a significant effort that was initiated at the suggestion of the ONR program manager but was not funded directly by ONR.

APPROACH

The performance metric of greatest interest was the combined turn-on and turn-off switching energy of the main and auxiliary devices. To obtain values for these losses, a physics-based state-space model of the IGBT was selected from the literature for use in a detailed simulation of the converter (see Appendix A). The particular state-space model selected was that of a non-punch-through IGBT [Hefner90a, Hefner90b, Hefner91], which correctly predicts the turn-on, turn-off and static characteristics of the device. This model is based on the equivalent circuit depicted on top of the IGBT cross section in Fig. 1. The state equations for this model are

$$\frac{dV_{bc}}{dt} = \frac{I_T - \frac{4D_p}{W^2}Q + \left(1+\frac{1}{b}\right)\left[\frac{C_{gd}}{C_{gs}+C_{gd}}I_g - I_{mos}\right]}{\left(1+\frac{1}{b}\right)\left[C_{dsj} + \frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}} + \frac{C_{bcj}}{3}\cdot\frac{Q}{Q_B}\right]} \tag{1}$$

$$\frac{dV_{gs}}{dt} = \frac{I_g}{C_{gs}+C_{gd}} + \frac{C_{gd}}{C_{gs}+C_{gd}}\cdot\frac{dV_{bc}}{dt} \tag{2}$$

$$\frac{dQ}{dt} = I_{mos} + \left(C_{dsj}+C_{gd}\right)\frac{dV_{bc}}{dt} - C_{gd}\frac{dV_{gs}}{dt} - \frac{Q}{\tau_{HL}} - \frac{Q^2}{Q_B^2}\cdot\frac{4N_B^2}{n_i^2}I_{sne} \tag{3}$$

where

b – Ambipolar mobility ratio.
C_{bcj} – Base-collector depletion capacitance (F).
C_{dsj} – Drain-source depletion capacitance (F).
C_{gd} – Gate-drain capacitance (F).
C_{gs} – Gate-source capacitance (F).
D_n, D_p – Electron, hole diffusivity (cm^2/s).
I_g – Gate current (A).
I_{mos} – MOSFET channel current (A).
I_{sne} – Emitter electron saturation current (A).
I_T – Anode current (A).
N_B – Base doping concentration (cm^{-3}).
n_i – Intrinsic carrier concentration (cm^{-3}).
Q – Instantaneous excess carrier base charge (C).

Q_B – Background mobile carrier base charge (C).
V_{bc} – Base-collector voltage (V).
V_{gs} – Gate-source voltage (V).
W – Quasi-neutral base width (cm).
τ_{HL} – Base high-level lifetime (s).

The state-space model of the IGBT was implemented in MATLAB using a file hierarchy that simplifies including the IGBT in various circuit topologies. In particular, at the circuit level, the non-linear state model is represented by a non-linear Thevenin equivalent circuit to facilitate its interconnection with passive circuit elements. The values of the voltage source and resistor of this Thevenin equivalent circuit are calculated by a subroutine based on the values of internal state variables of the transistor (accumulated charge, gate-source and base-collector voltages) and the gating voltage.

A state-space model for a power p-i-n diode that includes reverse recovery effect was also obtained from the literature [Lauritzen91]. The single state equation for this model is

$$\frac{dQ_M}{dt} = \frac{I_S\tau\left[\exp\left(\frac{v}{nV_T}\right)-1\right]-Q_M}{T_M} - \frac{Q_M}{\tau} = I_D - \frac{Q_M}{\tau} \tag{4}$$

where

I_D – Diode current (A).
I_s – Diffusion leakage current (A).
n – Emission coefficient.
Q_M – Charge in the base region (C).
T_M – Transit time (s).
v – Diode voltage (V).
V_T – Thermal voltage (V).
τ - Carrier recombination lifetime (s).

The state-space models of the IGBT and diode were tested initially using the simple hard switching circuit shown in Fig. 2. Typical voltage, current, and power waveforms obtained using this circuit are shown in Fig. 3. The portion of these waveforms near the switch transitions were then compared to results in [Hefner91] and [Lauritzen91]. This comparison showed good agreement, thereby confirming that the device models had been implemented properly. While discussing the voltage and current waveforms during switching, it is worthwhile to note that a major course of switching losses in the IGBT or other insulated-gate minority carrier devices is the presence of the

so-called current tail. This current tail is the result of diffusion and recombination of the excess carriers injected into the drift region via conductivity modulation in the on state. This current continues to flows as the voltage across the device rises during turn-off. The simultaneous presence of both current and voltage leads to power dissipation.

To establish one baseline for subsequent studies of the switching energy dissipated in a zero-current switching topology, a set of studies in which the value of the snubber capacitor in parallel with the IGBT was varied over a range of 2 to 200 nF was also conducted. The results of this study are shown in Fig. 4. At a typical value of 5 nF, the turn-off losses are 12 mJ, while the turn-on losses are 5 mJ. As expected, the turn-off losses decrease as the value of the snubber capacitor is increased, while the turn-on losses increase.

A second baseline was established using the IGBT and diode models in the Auxiliary Resonant Commutated Pole [DeDonker90]. This is a zero-voltage switching topology and is illustrated in Fig. 5. In this circuit, large snubber capacitors are used to maintain a low voltage across the IGBT during the tail interval. This decreases turn-off losses. To avoid potentially large turn-on losses, the auxiliary circuit is used to force the voltage of the on-coming main IGBT to zero prior to turn-on via a resonance between the auxiliary circuit inductor and the snubber capacitors. The precise switching strategy (sequence and times) to achieve this zero-voltage turn-on is described in [DeDonker90, Mayer98]. Typical waveforms for the inductor current and snubber capacitor voltages are shown in Fig. 6. The voltage, current, and instantaneous power waveforms for each of the four IGBTs is shown in Fig. 7. The total switching energy obtained from the simulation illustrated in Fig. 7 was 17.0 mJ, which is about the same as for the hard switching case. This is based on four devices rather than one device, however. Moreover, the gating sequence during the turn-on has not been completely optimized yet, thus the result can probably be improved.

Once the hard switched and ARCP baselines had been established, the IGBT and diode models were incorporated into a simulation of the so-called SSM (Shorter, Salberta, and Mayer) zero-current switching topology/strategy identified as a strong candidate in a prior study (see Appendix B). This topology is shown in Fig. 8. It represents a resonant bridge that provides zero-current turn-off but full-load turn-on.

This topology/strategy was chosen to minimize the so-called turn-around time associated with resonant switching.

The switching strategy was refined iteratively to establish a reasonable circuit response. The key variables of this response, the pole voltage, resonant inductor current, and resonant capacitor voltage are shown in Fig. 9. The voltage, current, and power waveforms for all four IGBTs are shown in Fig. 10. From the power waveforms, the total switching energy was found to be approximately 12 mJ.

CONCLUSIONS AND ON-GOING WORK

A framework for simulating zero-current (zero-voltage) switching circuits using a state-space model of the IGBT and power p-i-n diode has been established. This simulation capability using MATLAB can compliment the use of commercial circuit simulation tools such as Saber by allowing for rapid prototyping of physics-based models. The models of the IGBT and diode presently used were taken from the literature, but work is underway to derive enhanced models. A hardware circuit for validating the models is also being considered.

The models and simulation code/methodology developed in this project will be transferred to NSWCCD/P starting with a day-long tutorial on component modeling and simulation scheduled for March 8, 2000.

REFERENCES

[DeDonker90] DeDoncker, R. W. and J. P. Lyons, 1990, "The Auxiliary Resonant Commutated Pole Converter," IEEE-IAS Conference Record, pp.1228-1235.

[Hefner90a] Hefner, A. J., Jr., 1990, "An improved understanding for the transient operation of the power insulated gate bipolar transistor (IGBT)", IEEE Trans. Power Electron., vol. 5, no. 4, 459-468.

[Hefner90b] Hefner, A. J., Jr., 1990, "Analytical modeling of device-circuit interactions for the power insulated gate bipolar transistor (IGBT)", IEEE Trans. Ind. Appl., vol. 26, no. 6, 995-1005.

[Hefner91] Hefner, A. J., Jr., 1991, "An investigation of the drive circuit requirements for the power insulated gate bipolar transistor (IGBT)", IEEE Trans. Power Electron., vol. 6, no. 2, 208-219.

[Lauritzen91] Lauritzen. P. O. and Cliff L. Ma, 1991, "A simple diode model with reverse recovery", IEEE Trans. Power Electron., vol. 6, no. 2, 188-191.

[Mayer98] Mayer, J. S., 1998, Modeling and Simulation of a Motor Controller and Permanent Magnet Motor, Final Technical Report for Contract N00039-97-D-0042.

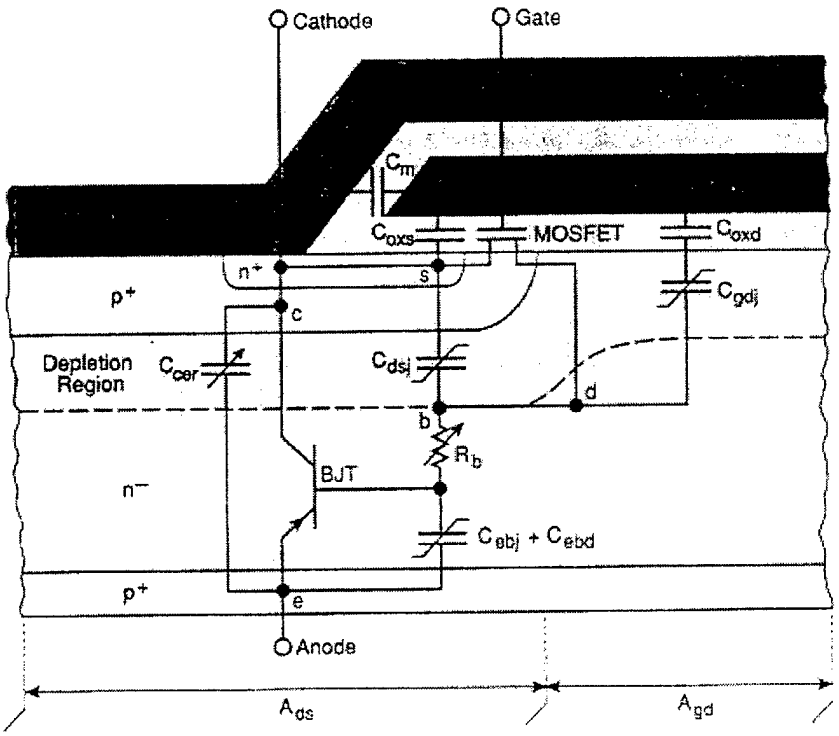

Fig. 3. Configuration of MOSFET and bipolar equivalent circuit components superimposed on schematic of one-half of symmetric IGBT cell.

Figure 1. Cross section of a non-punch-through IGBT [Hefner91].

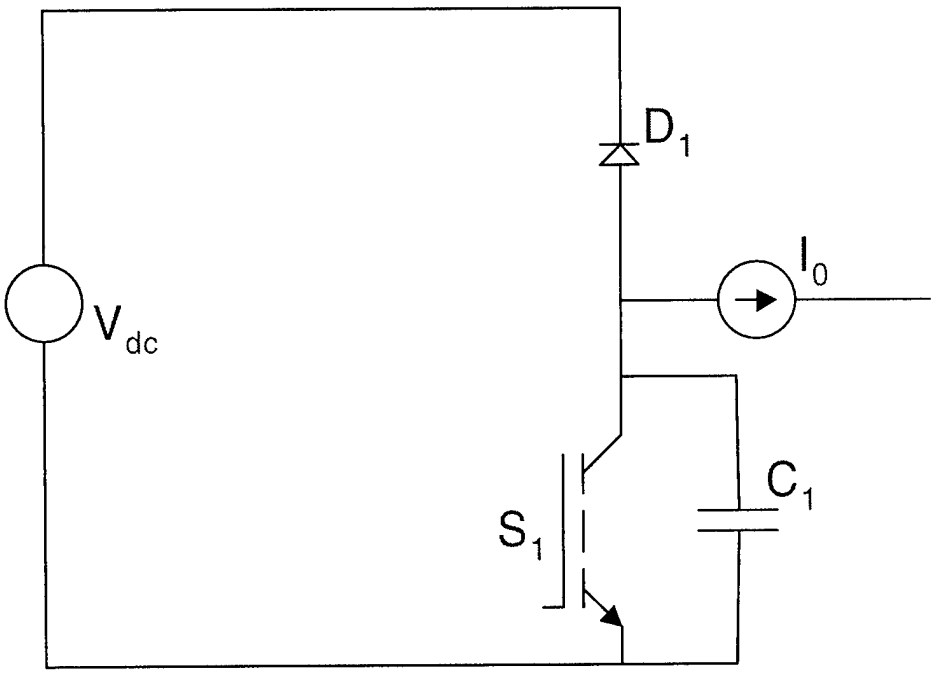

Figure 2. Schematic of circuit used to study hard switching characteristics.

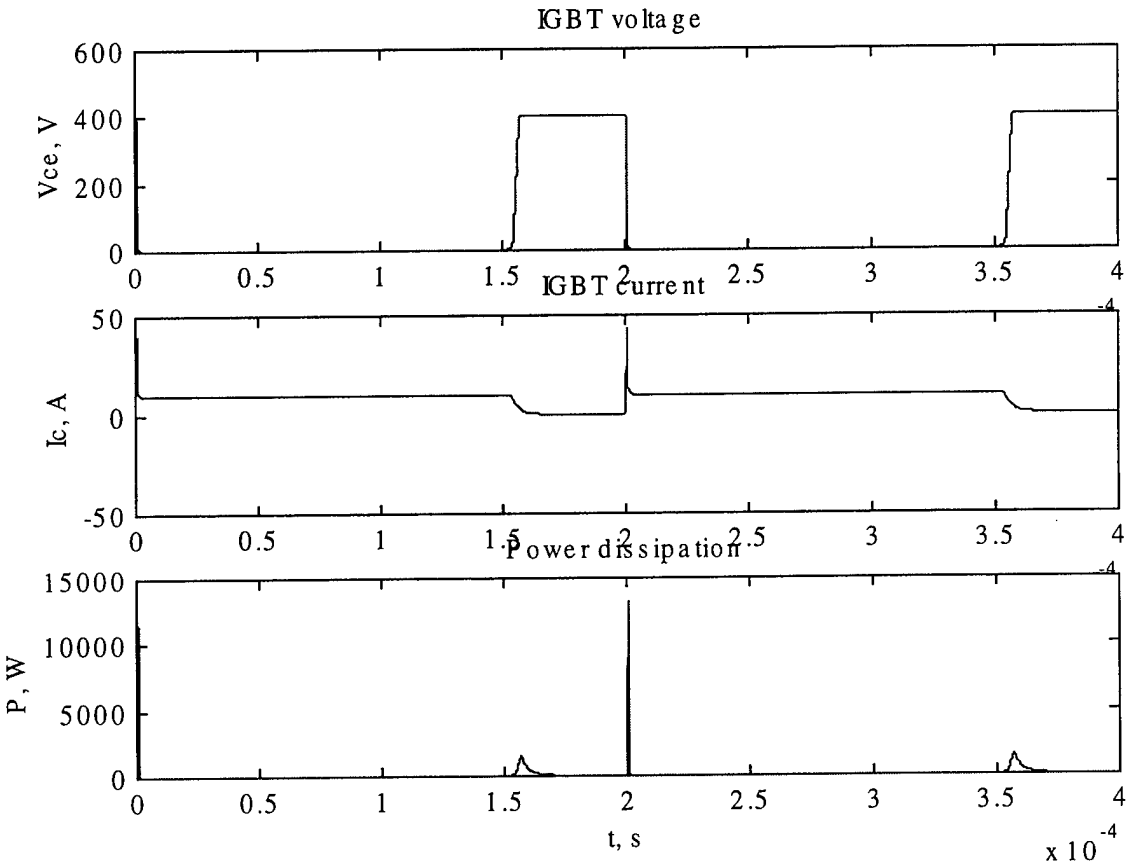

Figure 3. Voltage, current, and power waveforms for two hard-switched cycles.

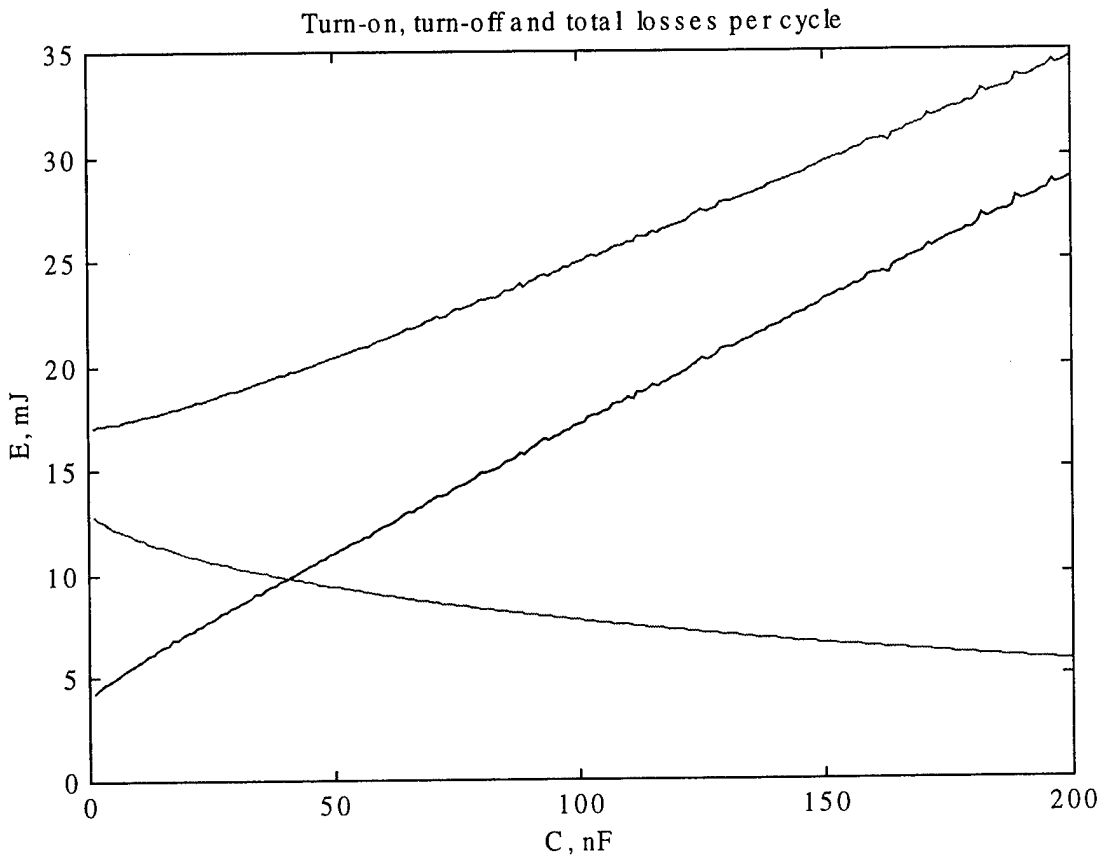

Figure 4. Plots of turn-on, turn-off, and total energy loss as a function of snubber capacitor value for hard switching.

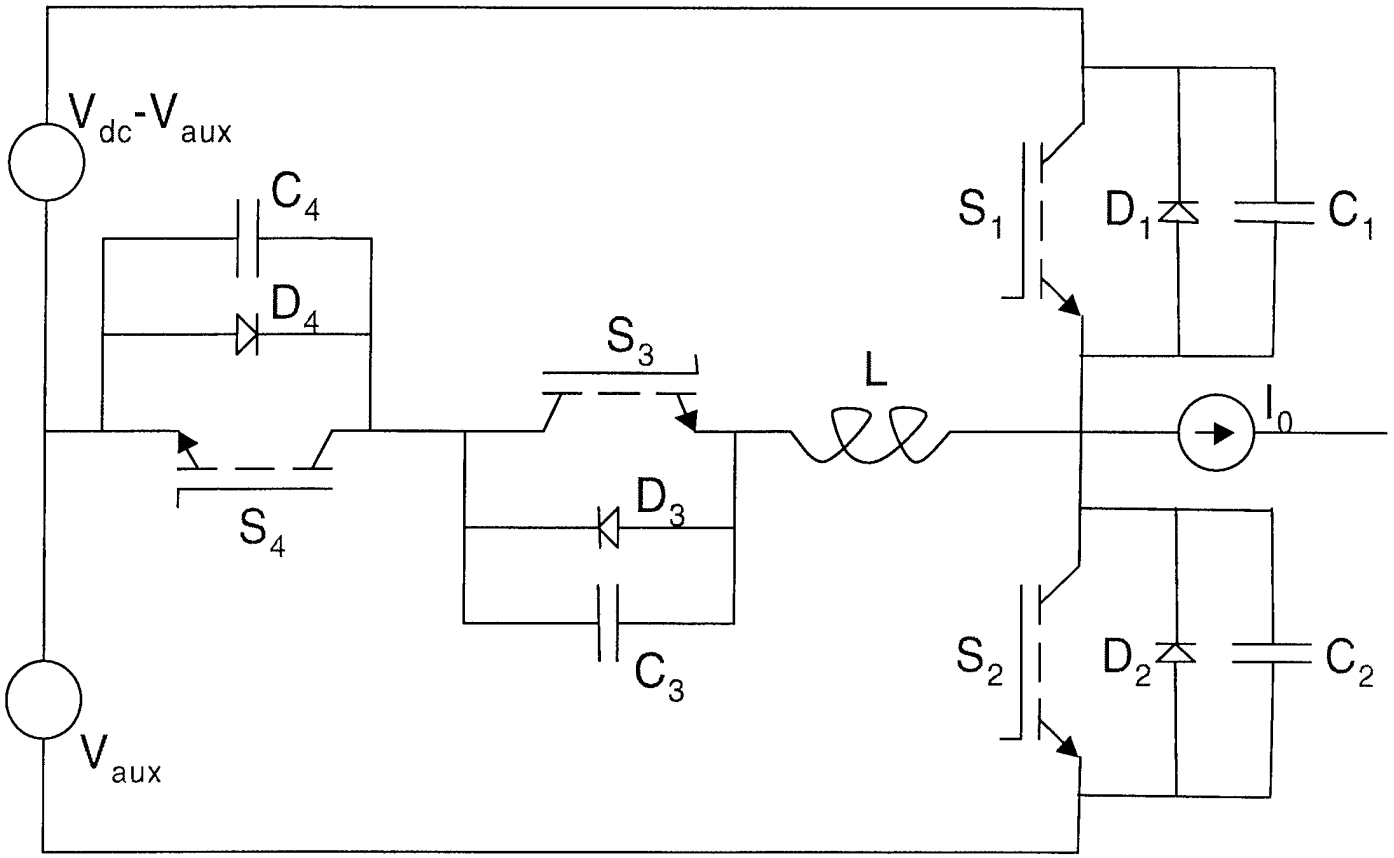

Figure 5. Schematic of ARCP circuit.

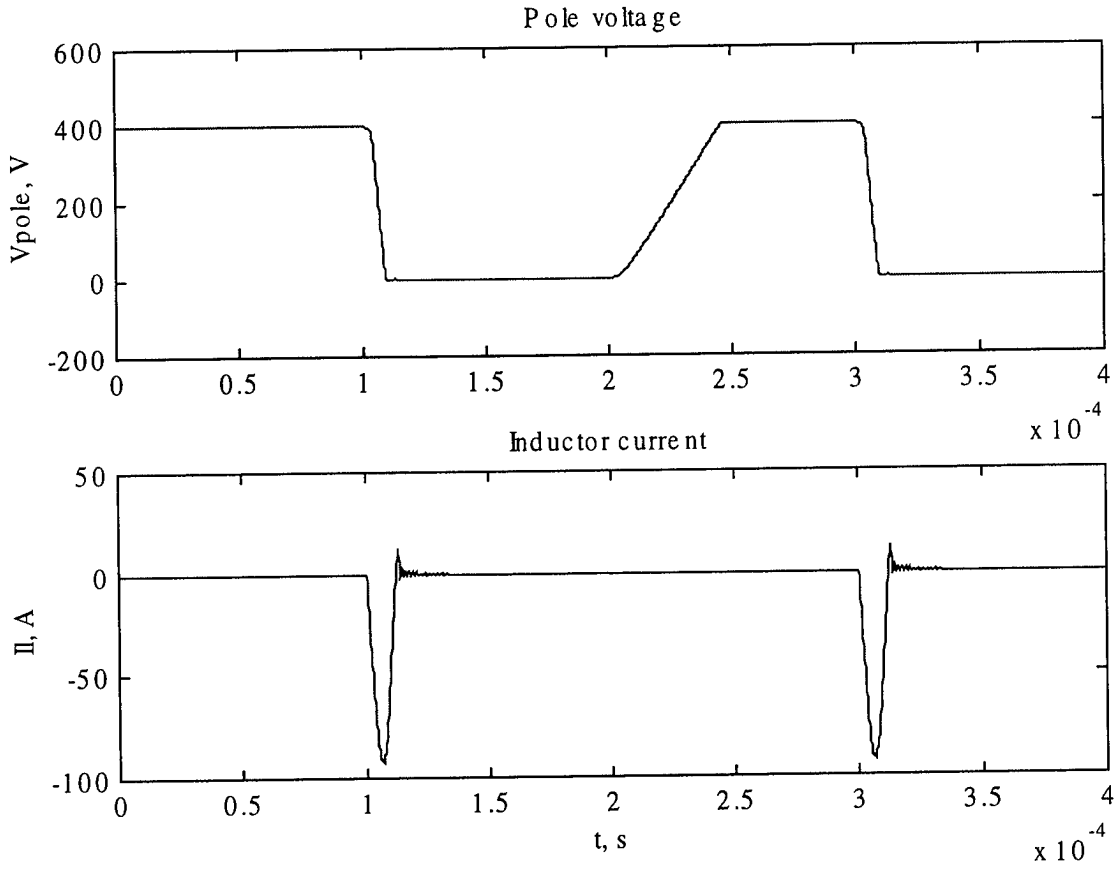

Figure 6. Pole voltage and auxiliary current waveforms for the ARCP.

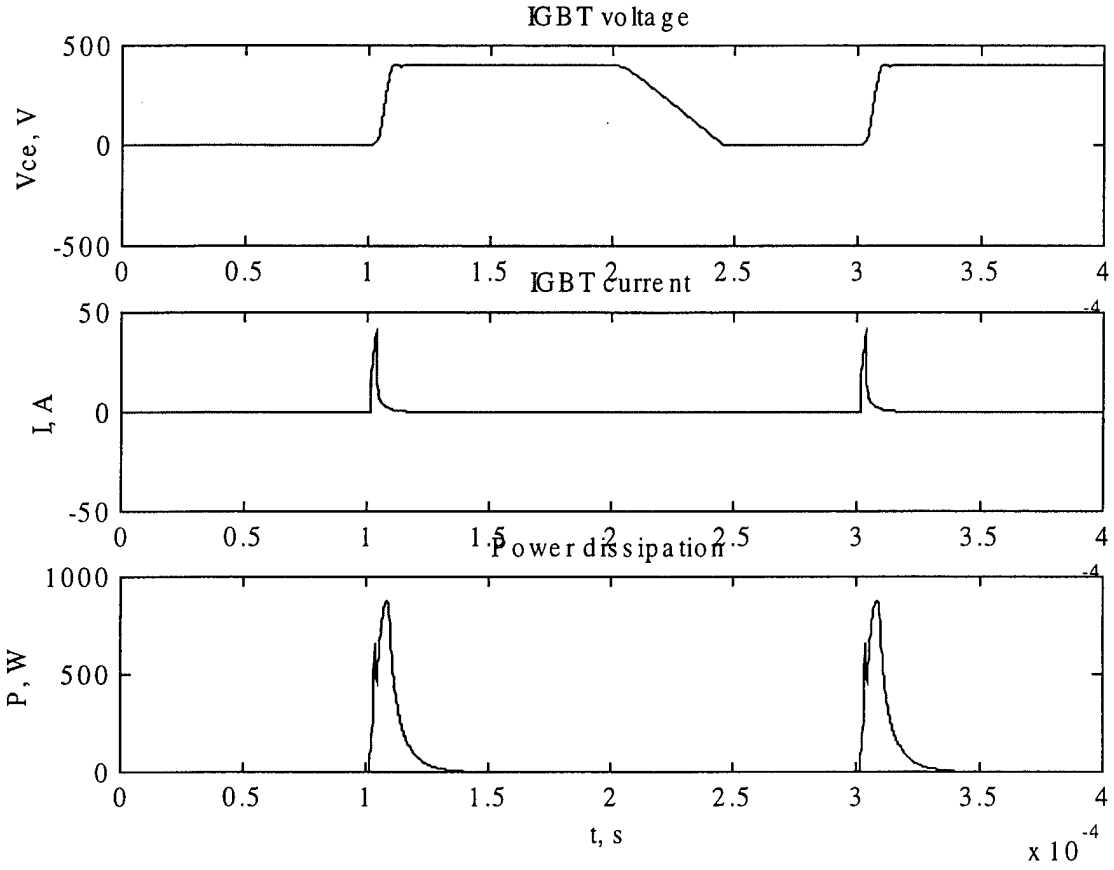

Figure 7a. Voltage, current, and power waveforms for switch S1 in the ARCP.

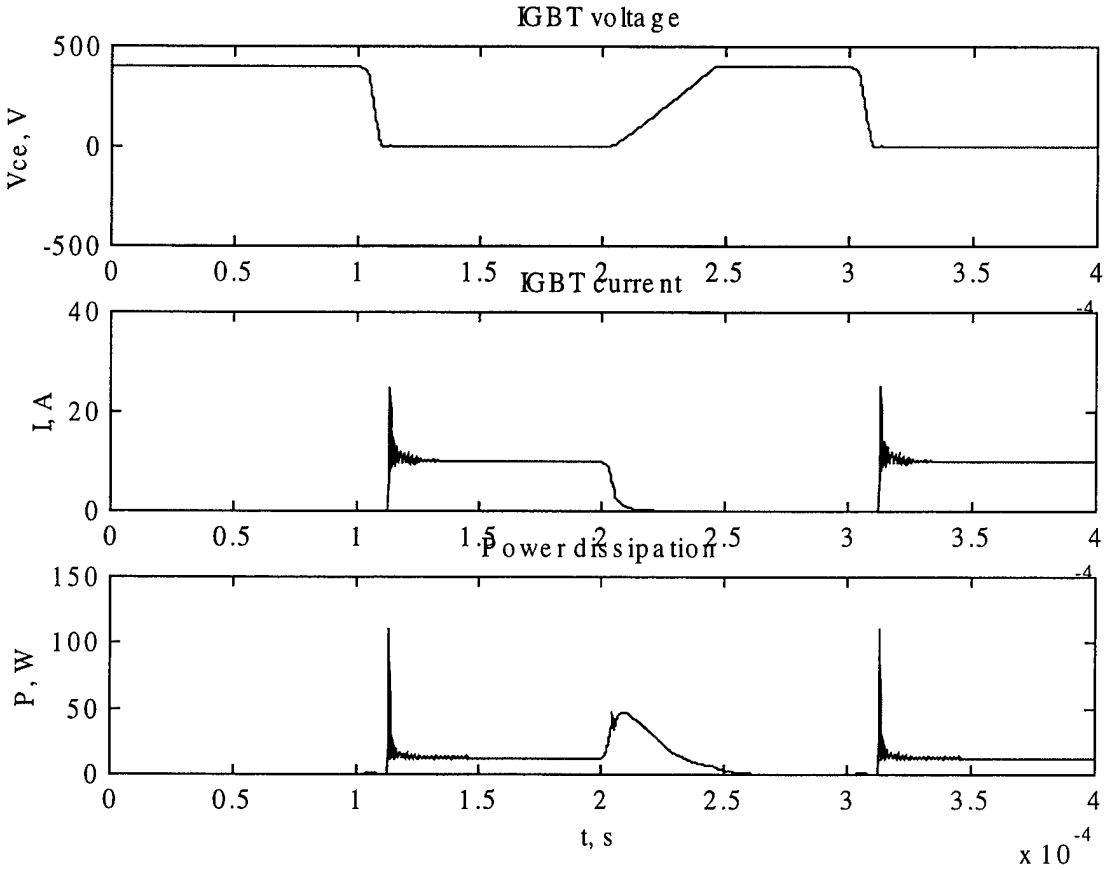

Figure 7b. Voltage, current, and power waveforms for switch S2 in the ARCP.

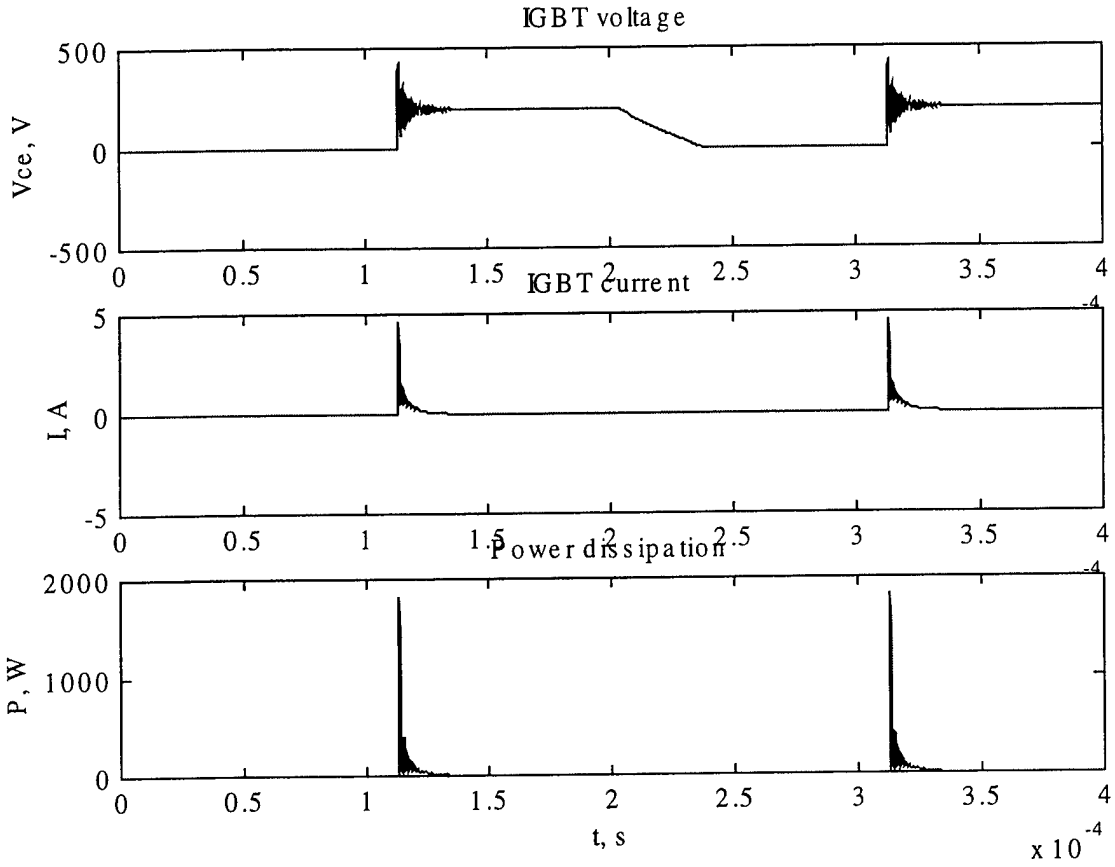

Figure 7c. Voltage, current, and power waveforms for switch S3 in the ARCP.

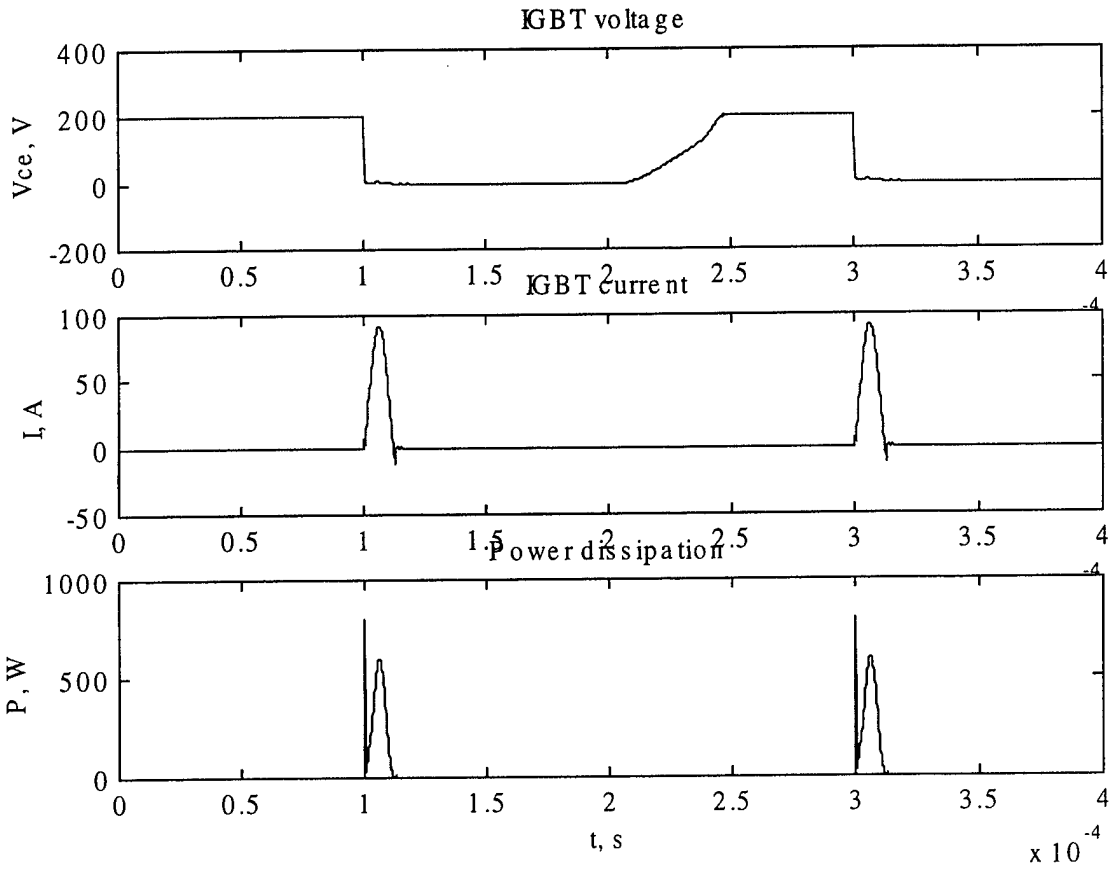

Figure 7d. Voltage, current, and power waveforms for switch S4 in the ARCP.

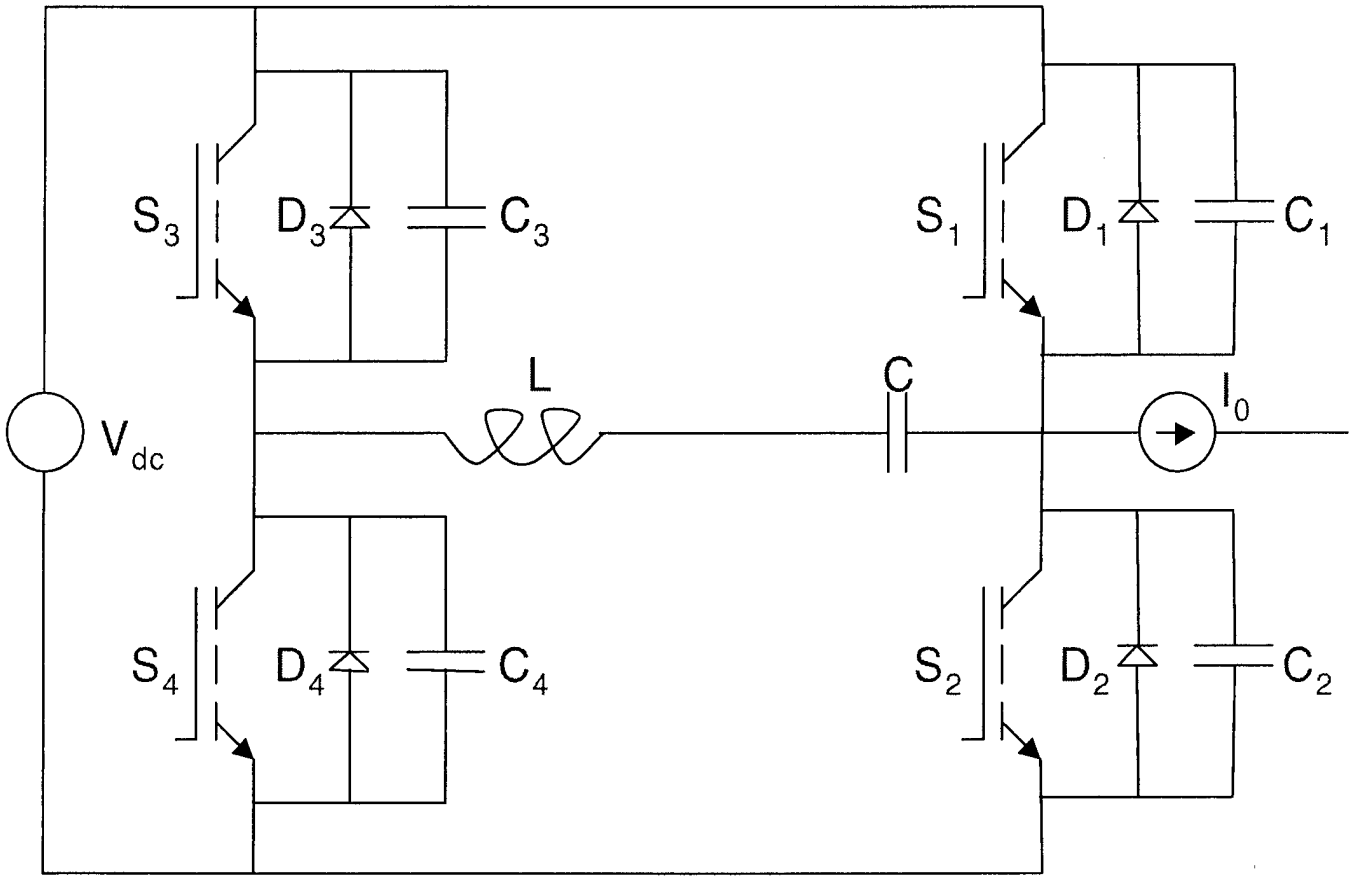

Figure 8. Schematic of SSM circuit.

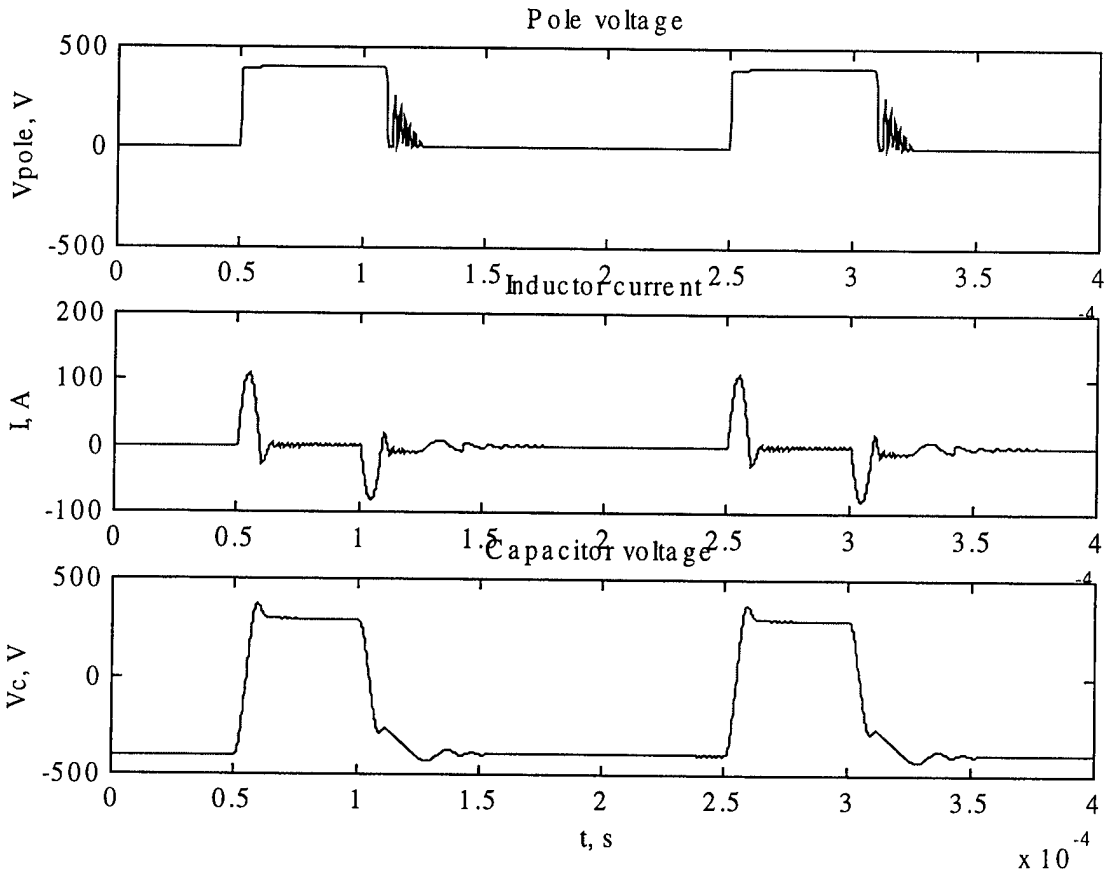

Figure 9. Pole voltage, resonant inductor current, and resonant capacitor voltage waveforms for the SSM.

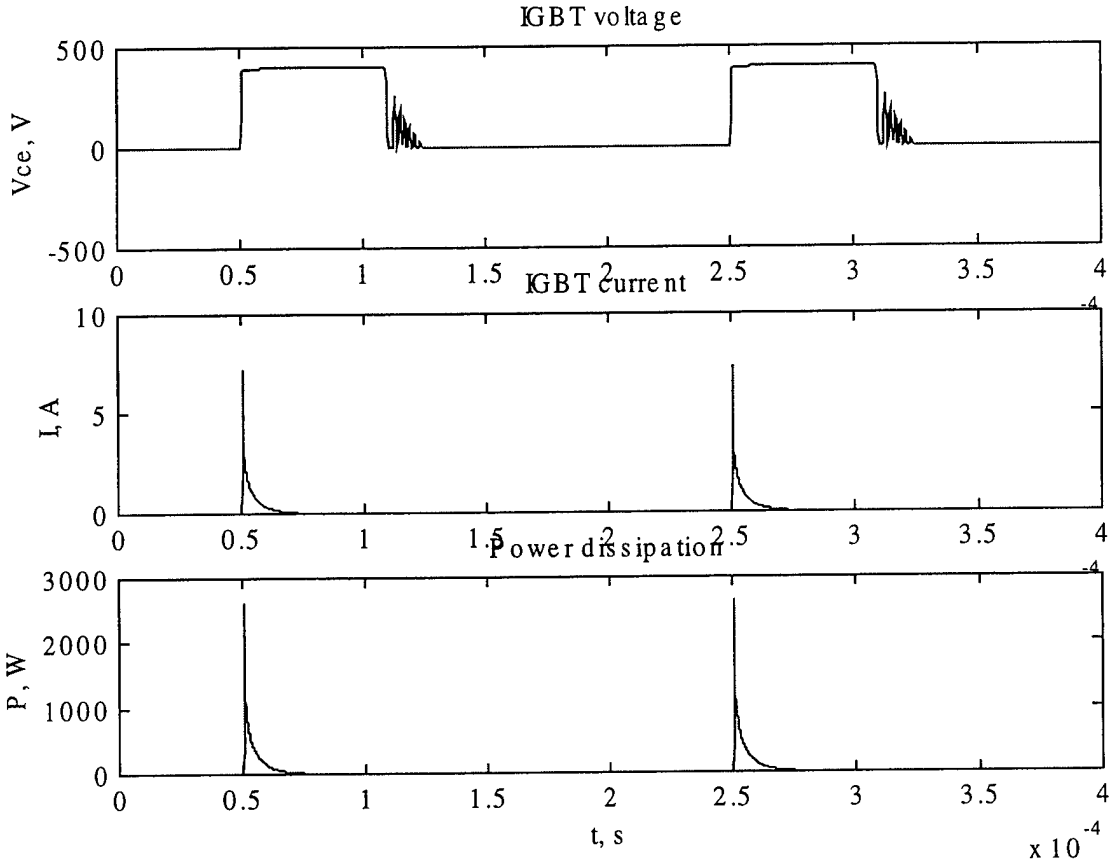

Figure 10a. Voltage, current, and power waveforms for switch S1 in the SSM.

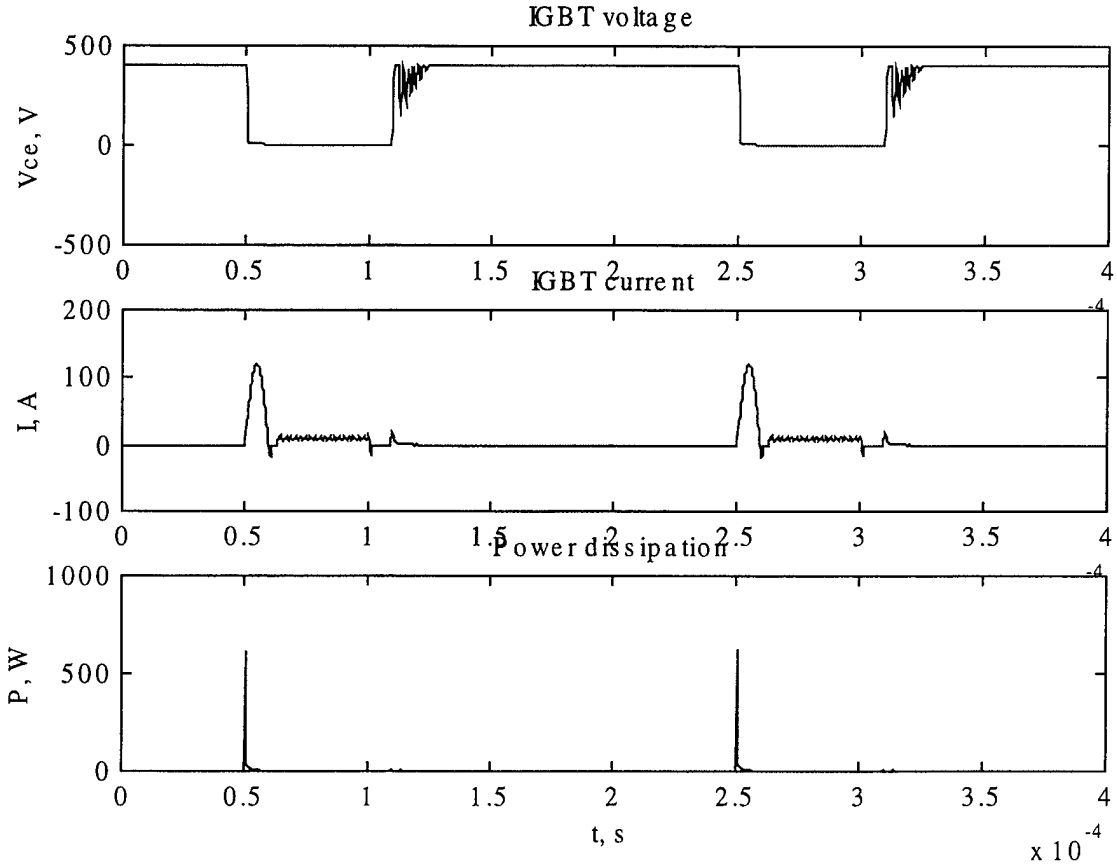

Figure 10b. Voltage, current, and power waveforms for switch S2 in the SSM.

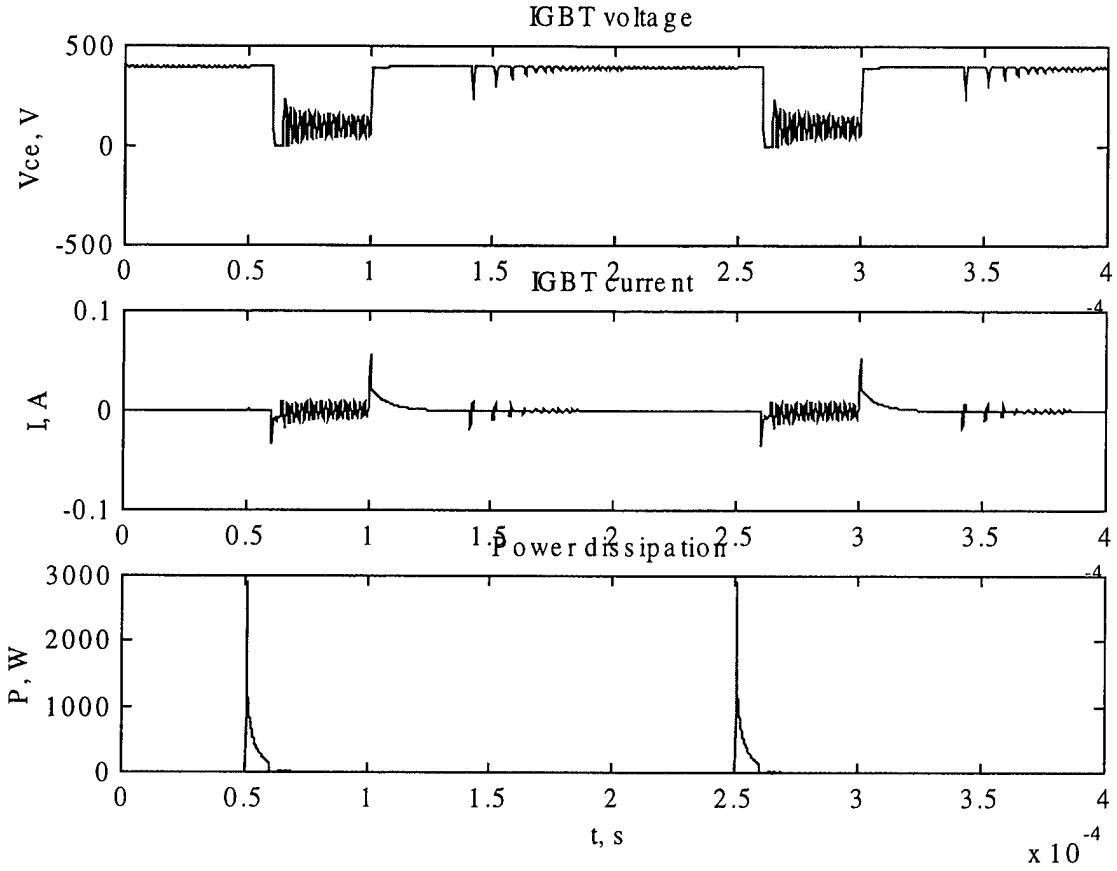

Figure 10c. Voltage, current, and power waveforms for switch S3 in the SSM.

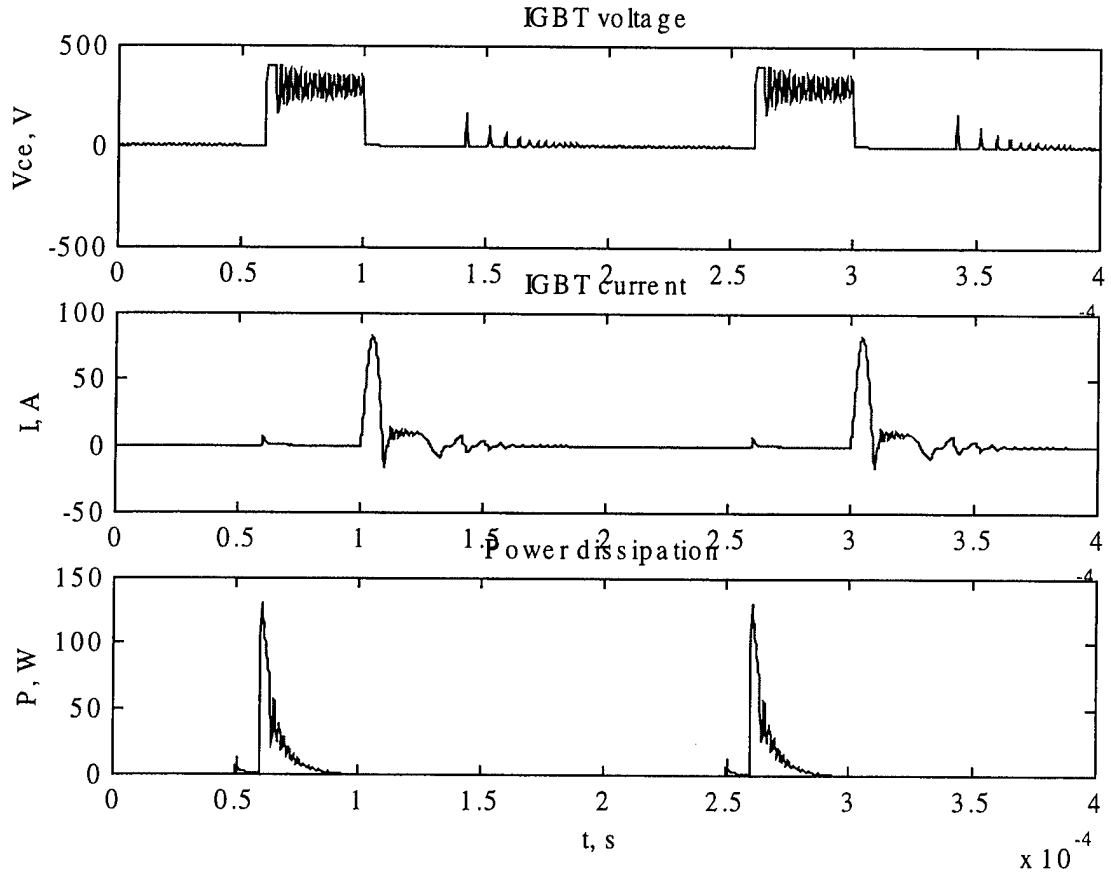

Figure 10d. Voltage, current, and power waveforms for switch S4 in the SSM.

APPENDIX A

BIBLIOGRAPHY ON MODELING SEMICONDUCTOR DEVICE DYNAMICS

General Topics

Authors	Title	Year	Source	Notes
B. Allard, H. Morel, and J.P. Chante	"State-variable modeling of high-level injection regions in power devices. Application to power system simulation."	1992	IEEE PESC Proceedings, v.2, 885-892	Describes the principles of building a power device model in terms of state variables and bond graphs; considers BJT as an example.
C.L. Ma, P.O. Lauritzen, P.-Y. Lin, I. Budihardjo, and J. Sigg	"A systematic approach to modeling of power semiconductor devices based on charge control principles"	1994	IEEE PESC Proceedings, v.1, 31-37	Provides a description of basic principles of building a charge control based model for power devices; gives examples and references.
Ph. Leturcq, M.O. Berraies, J.-P. Laur and P. Austin	"Full dynamic power bipolar device models for circuit simulation"	1998	IEEE PESC Proceedings, v.2, 1695-1703	Suggests an approach to modeling several interacting semiconductor switches.

P-N Junctions

Authors	Title	Year	Source	Notes
E.M. Pell	"Recombination rate in germanium by observation of pulsed reverse characteristic"	1953	Phys. Rev., 90, 2, 278-279	Gives approximate solution for diode switching as a way to find recombination time in germanium
R.G. Shulman and M.E. McMahon	"Recovery currents in germanium p-n junction diodes"	1953	Journ. of Appl. Phys., 24, 10, 1267-1272	Provides an explanation of the current tail during turn-off
R.H. Kingston	"Switching time in junction diodes and junction transistors"	1954	Proceedings of the IRE, 829-834	Gives approximate solution for the recovery time of a diode assuming constant current conditions.
B. Lax and S.F. Neustadter	"Transient response of a p-n junction"	1954	Journ. of Appl. Phys., 25, 9, 1148-1154	Gives an exact solution for the diode transient response solving the diffusion equation.
N.T. Jones, R.H. Kingston, and S.F. Neustadter	"Anomalous forward switching transient in p-n junction diodes"	1955	Journ. of Appl. Phys., 26, 2, 210-213	Explains the delay in turn-on transient for p-n junction diodes

Thyristor Structures

Authors	Title	Year	Source	Notes
R.L. Longini and J. Melngailis	"Gated turn-off of four-layer switch"	1963	IEEE Trans. El. Dev., ED-10, 3, 178-185	Describes the process of gated turn-off for thyristor structure.
E.D. Wolley	"Gate turn-off in p-n-p-n devices"	1966	IEEE Trans. El. Dev., ED-13, 7, 590-597	Suggests a simple 2-D model for gated turn-off of a p-n-p-n device
V.V. Togatov	"The theory of the turn-off process of the p-n-p-n structure"	1973	Radio Eng. and Electron. Phys., 17, 1, 117-121	Gives an analytical model for the thyristor turn-off.
A.A. Jaecklin	"The first dynamic phase at turn-on of a thyristor"	1976	IEEE Trans. El. Dev., ED-23, 8, 940-944	A simple theoretical model for thyristor turn-on is given.
V.V. Togatov	"Calculation of the turn-on process in a quasilinear model of the p-n-p-n structure"	1977	Radio Eng. and Electron. Phys., 22, 5, 102-107	A method is proposed for calculating the turn-on process in thyristors.
M.S. Adler and V.A.K. Temple	"The dynamics of the thyristor turn-on process"	1980	IEEE Trans. El. Dev., ED-27, 2, 483-494	Modeling results on thyristor turn-on are described
V.A.K. Temple	"MOS controlled thyristors"	1984	IEDM Tech. Digest, 282-285	Describes the conception and design of the new device (MCT).
V.A.K. Temple and W. Tantraporn	"Effect of temperature and load on MCT turn-off capability"	1986	IEDM Tech. Digest, 118-121	The first study on turn-off in MCTs.
T.M. Jahns, R.W.A.A. De Doncker, J.W.A. Wilson, V.A.K. Temple, and D.L. Watrous	"Circuit utilization characteristics of MOS-controlled thyristors"	1991	IEEE Trans. Ind. Appl., 27, 3, 589-597	Discusses the experimental data on switching and other characteristics of MCTs
T. Lee, D.S. Zinger, and M.E. Elbuluk	"Modeling, simulation and testing of MCT under zero voltage resonant switching"	1991	Ind. Electronics Conf. Proceedings, v.1 , 341-346	Presents a PSPICE circuit model for MCTs.
R.W.A.A. De Doncker, T.M. Janhs, A.V. Radun, D.L. Watrous, and V.A.K. Temple	"Characteristics of MOS-controlled thyristors under zero-voltage soft-switching conditions"	1992	IEEE Trans. Ind. Appl., 28, 2, 387-394	Summarizes the key MCT characterization results in relation to zero voltage switching.
C.L. Ma, P.O. Lauritzen, P.	"A physically-based lumped charge SCR	1993	IEEE PESC Proceedings,	Gives a lumped-charge model for thyristor type structures.

Turkes, and H.J. Mattausch	model"		v.1, 53-59	
M.S. Shekar and B.J. Baliga	"Modeling the on-state characteristics of the emitter switched thyristor"	1994	Solid-State Electron., 37, 7, 1403-1412	Develops an analytical model for the on-state operation of EST
M. Trivedi, S. Pendharkar, and K. Shenai	"Switching characteristics of MCTs and IGBTs in power converters"	1996	IEEE Trans. El. Dev., 43, 11, 1994-2003	2-D simulation (ATLAS) of transient behavior of IGBTs and MCTs. Comparison to experimental results.
Z. Hossain, E.X. Yang, V.A.K. Temple, C.L. Ma, and K.J. Olejniczak	"An MCT circuit model using the lumped-charge modeling technique"	1996	IEEE PESC Proceedings, v.1, 23-28	Gives a lumped-charge model for MCTs.
M. Breil, J.-L. Sanchez, P. Austin, and J.-P. Laur	"Turn-off performance comparison of self-firing MOS-thyristor devices for ZVS applications"	1998	IEEE Bipolar/BiCMOS Circ. and Tech. Meeting Proc., 53-56	2-D simulation (PISCES) is used to suggest design improvements for better turn-off performance

Bipolar Devices

Authors	Title	Year	Source	Notes
G.M. Kull, L.W. Nagel, S.-W. Lee, P. Lloyd, E.J. Prendergast, and H. Dirks	"A unified circuit model for bipolar transistor including quasi-saturation effects"	1985	IEEE Trans. El. Dev., ED-32, 6, 1103-1113	Suggests a model describing static behavior and charge storage effects. Recombination is not considered.
C. Xu and D. Schroder	"A power bipolar junction transistor model describing static and dynamic behavior"	1992	IEEE Trans. Power Electron., 7, 4, 734-740	Suggests a new model extending the charge-control approach by solving the diffusion equation under approximation dp/dt=p/T(t)
M. Bayer, R. Kraus, and K. Hoffmann	"A precise model for the DC and transient characteristics of BJTs"	1994	IEEE PESC Proceedings, v.1, 64-68	An exact solution of diffusion equation is given when the time derivative is approximated as a function of boundary values and x.
N. Talwakar, P.O. Lauritzen, B. Fatemizadeh, D. Periman, and C.L. Ma	"A power BJT model for circuit simulation"	1996	IEEE PESC Proceedings, v.1, 50-55	Gives a 1-D model based on the lumped-charge approach
M. Trivedi, R. Vijayalakshmi, K. Shenai, and B. Hesterman	"Improved capacitance model for power bipolar transistor turn-off performance"	1998	IEEE PESC Proceedings, v.2, 1214-1218	Gives physically based expression for capacitance during the switching of any type.
K. Datta and M. Jagadesh Kumar	"A simple hole scattering length model for the solution of charge transport in bipolar transistors"	1999	IEEE Trans. El. Dev., 46, 6, 1186-1188	Proves that hole scattering length is energy-independent; has references on BJT analytical treatment.

IGBT

Authors	Title	Year	Source	Notes
H. Yilmaz, J.L. Benjamin, R.F. Dyer, Jr., L.-S. S. Chen, W.R. Van Dell, and G.C. Pifer	"Comparison of the punch-through and non-punch-through IGT structures"	1986	IEEE Trans. Ind. Appl., IA-22, 3, 466-470	Shows the differences between the punch-through and non-punch-through IGBTs.
D.-S. Kuo, C. Hu, and S.P. Sapp	"An analytical model for the power bipolar-MOS transistor"	1986	Solid-State Electron., 29, 12, 1229-1237	Gives the first 1-D model for IGBTs using a quasi-static approximation for transient analysis.
A.J. Hefner, Jr. and D.L. Blackburn	"An analytical model for the steady-state and transient characteristics of the power IGBT"	1988	Solid-State Electron., 31, 10, 1513-1532	Describes the first non-quasi-static 1-D IGBT model based on ambipolar approach.
R. Rangan, D.Y. Chen, J. Yang and J. Lee	"Application of insulated gate bipolar transistors to zero-current switching converters"	1989	IEEE Trans. Power Electron., 4, 1, 2-7	Discusses the behavior of IGBTs in zero-current switches, including turn-on and turn-off power losses, dv/dt, etc.
A.J. Hefner, Jr.	"An improved understanding for the transient operation of the power insulated gate bipolar transistor (IGBT)"	1990	IEEE Trans. Power Electron., 5, 4, 459-468	Shows that a non-quasi-static model, considering the change in base width, must be used in order to accurately simulate IGBT transient behavior.
A.J. Hefner, Jr.	"Analytical modeling of device-circuit interactions for the power insulated gate bipolar transistor (IGBT)"	1990	IEEE Trans. Ind. Appl., 26, 6, 995-1005	Based on the previously developed model, the turn-off transient behavior of IGBTs is simulated for a series resistor-inductor load in order to determine SOA.
A.J. Hefner, Jr.	"An investigation of the drive circuit requirements for the power insulated gate bipolar transistor (IGBT)"	1991	IEEE Trans. Power Electron., 6, 2, 208-219	Completes previously developed model by including a simple MOSFET description that permits to correctly describe turn-on.
A.J. Hefner, Jr. and D.M. Diebolt	"An experimentally verified IGBT model implemented in the Saber circuit simulator"	1991	IEEE PESC Proceedings, v.1, 10-19	Repeats the equations of the previously developed model and shows how to implement them in a circuit simulator.
C.S. Mitter, A.R. Hefner, Jr., D.Y. Chen and F.C. Lee	"Insulated Gate Bipolar Transistor (IGBT) modeling using IG-Spice"	1993	IEEE Trans. Ind. Appl., 30, 1, 24-33	Repeats the equations of Hefner's model and shows how to implement them in IG-Spice.
R. Kraus and K.	"An analytical model of	1993	IEEE Internat.	Suggests a model for IGBTs

Hoffmann	IGBTs with low emitter efficiency"		Symp. on Power Semicond. Dev. and ICs, 30-34	alternative to Hefner's model that is more difficult to write in state variable form.
H. Dettmer, U. Krumbein, H. Lendenmann, S. Muller, W. Fichtner, F. Bauer, K. Lilja, and T. Stockmeier	"A comparison of the switching behavior of IGBT and MCT power devices"	1993	IEEE Internat. Symp. on Power Semicond. Dev. and ICs, 54-59	Discusses the dynamic avalanche phenomena in IGBTs and MCTs and how it affects the transient characteristics of these two devices
S. Lefebvre, F. Forest, F. Calmon, and J.P. Chante	"Turn-off analysis of the IGBT used in ZCS mode"	1994	IEEE Internat. Symp. on Power Semicond. Dev. and ICs, 99-104	1-D (GIGA) and 2-D (MEDICI) simulations; comparison to experimental results; simple 1-D model.
K. Wang, F.C. Lee, G. Hua, and D. Borojevic	"A comparative study of switching losses of IGBTs under hard-switching, ZVS and ZCS"	1994	IEEE PESC Proceedings, v.2, 1196-1204	Switching losses of IGBTs are studied experimentally. The paper shows the advantages of soft-switching techniques.
A.J. Hefner, Jr.	"Modeling buffer layer IGBTs for circuit simulation"	1995	IEEE Trans. Power Electron., 10, 2, 111-123	A physical model for punch-through IGBTs is given based on the previous non-punch-through model
I. Widjaja, A. Kurnia, K. Shenai, and D. Divan	"Switching dynamics of IGBTs in soft-switching converters"	1995	IEEE Trans. El. Dev., 42, 3, 445-454	2-D simulation (probably ATLAS) of IGBTs under soft-switching conditions; comparison to experimental data.
F. Urdea and G.A.J. Amaratunga	"A unified analytical model for the carrier dynamics in trench insulated gate bipolar transistors"	1995	IEEE Internat. Symp. on Power Semicond. Dev. and ICs, 190-195	Gives a physically-based on-state model for trench IGBTs
M. Trivedi, S. Pendharkar, and K. Shenai	"Switching characteristics of MCTs and IGBTs in power converters"	1996	IEEE Trans. El. Dev., 43, 11, 1994-2003	2-D simulation (ATLAS) of transient behavior of IGBTs and MCTs. Comparison to experimental results.
A. Elasser, V. Parthasarathy, and D. Torrey	"A study of the internal device dynamics of punch-through and non-punch-through IGBTs under zero-current switching	1997	IEEE Trans. Power Electron., 12, 1, 21-35	2-D simulation (MEDICI) for internal carrier dynamics in IGBTs during switching; focus on circuit performance.

M. Trivedi and K. Shenai	"Modeling the turn-off of IGBTs in hard- and soft-switching applications"	1997	IEEE Trans. El. Dev., 44, 5, 887-893	Gives a 1-D physical model of switching based on the assumption of constant charge distribution in the base (except recombination).
S. Musumeci, A. Raciti, A. Testa, A. Galluzzo and M. Melito	"Switching behavior improvement of insulated gate-controlled devices"	1997	IEEE Trans. Power Electron., 12, 4, 645-653	Suggests gate-driving techniques for power loss reduction during the MOS turn-off stage; more useful for MOSFETs than IGBTs.
F. Urdea and G.A.J. Amaratunga	"An on-state analytical model for the trench insulated gate bipolar transistor (TIGBT)"	1997	Solid-State Electron., 41, 8, 1111-1118	Gives a physically-based on-state model for trench IGBTs
M. Trivedi, K. Shenai, and E. Larson	"Critical evaluation of IGBT performance in zero current switching environment"	1997	IEEE IAS Annual Meeting Proceedings, v.2, 989-993	2-D simulation (ATLAS) of internal carrier dynamics of IGBT under zero current switching conditions.
Y.C. Gerstenmaier and M. Stoisiek	"Switching behavior of high voltage IGBTs and its dependence on gate-drive"	1997	IEEE Internat. Symp. on Power Semicond. Dev. and ICs, 105-108	The turn-on switching is considered for two IGBT types based on experimental data and MEDICI simulations.
J. Yamashita, N. Soejima, and H. Haruguchi	"A novel effective switching loss estimation of non-punchthrough and punchthrough IGBTs"	1997	IEEE Internat. Symp. on Power Semicond. Dev. and ICs, 109-112	Estimates switching losses for PT and NPT IGBTs
Y.C. Gerstenmaier and M. Stoisiek	"Switching behavior of high voltage IGBTs and its dependence on gate-drive"	1997	IEEE Internat. Symp. on Power Semicond. Dev. and ICs, 105-108	The turn-on switching is considered for two IGBT types based on experimental data and MEDICI simulations.
N. Thapar and B.J. Baliga	"An experimental evaluation of the on-state performance of trench IGBT designs"	1998	Solid-State Electron., 42, 5, 771-776	Compares the experimental results for non-self-aligned and self-aligned trench IGBTs; shows the superiority of the former.
D.W. Berning and A.J. Hefner, Jr	"IGBT model validation"	1998	IEEE Ind. Appl. Magazine, Nov./Dec., 23-34	Suggests a circuit for IGBT models validation. Has information and references on previous Hefner's work.
K. Sheng, S.J.	"A new analytical IGBT	1999	IEEE Trans.	Gives a new model including

Finney, and B.W. Williams	model with improved electrical characteristics"		Power Electron., 14, 1, 98-107	2-D effects in the forward conduction of IGBTs.
S. Lefebvre and F. Miserey	"Analysis of CIC NPT IGBTs turn-off operation for high switching current level"	1999	IEEE Trans. El. Dev., 46, 5, 1042-1049	Analyses the effects related to avalanche generation for snubberless turn-off; gives a 1-D analytical model similar to Hefner's.
M. Trivedi and K. Shenai	"Internal dynamics of IGBT under zero-voltage and zero-current switching conditions"	1999	IEEE Trans. El. Dev., 46, 6, 1274-1282	2-D simulation (ATLAS) for internal carrier dynamics in IGBTs during switching.
A. Ramamurthy, S. Sawant, and B.J. Baliga	"Modeling the dV/dt of the IGBT during inductive turn-off"	1999	IEEE Trans. Power Electron., 14, 4, 601-606	Suggests a model for the turn-off which best virtue is its simplicity.
A.N. Githiari, B.M. Gordon, R.A. McMahon, Z.-M. Li, and P.A. Mawby	"A comparison of IGBT models for use in circuit design"	1999	IEEE Trans. Power Electron., 14, 4, 607-614	Compares the models of Hefner and Kraus with each other and with the experimental data; shows the good agreement of all three.

Other Devices

Authors	Title	Year	Source	Notes
N. Thapar and B.J. Baliga	"The accumulated channel driven bipolar transistor (ACBT)"	1997	IEEE El. Dev. Lett., 18, 5, 1997	Proposes a new three-terminal power switch. The experimental results show the superiority of this device comparing to other existing switches.
N. Thapar and B.J. Baliga	"Influence of the collector resistance on the performance of accumulation channel driven bipolar transistor"	1998	Solid-State Electron., 42, 9, 1697-1703	Studies the mechanism limiting the performance of ACBTs.
N. Thapar and B.J. Baliga	"Analytical model for the threshold voltage of accumulated channel MOS-gate devices"	1998	Solid-State Electron., 42, 11, 1975-1979	Derives the equation for the threshold voltage of ACBTs in terms of device fabrication parameters.
N. Thapar and B.J. Baliga	"Enhancing the maximum controllable current density of the accumulated channel driven bipolar transistor"	1999	Solid-State Electron., 43, 3, 395-402	Explains the physical mechanism responsible for current reduction in ACBTs and shows how it can be avoided by changing the fabrication process.

APPENDIX B
PREVIOUS REPORT ON THE ANALYSIS OF ZERO-CURRENT SWITCHING TOPOLOGIES AND STRATEGIES FOR THE POWER ELECTRONIC BUILDING BLOCK

This appendix contains the full text of a report on the previous analysis of four zero-current switching topologies and strategies. It is included for archival purposes, because the analysis was conducted at the suggestion of the ONR program manager.

EXECUTIVE SUMMARY

This report documents work performed at The Pennsylvania State University (PSU) in support of future PEBB development at the Naval Surface Warfare Center, Carderock Division, Philadelphia Detachment (NSWCCD/P). Work at PSU has focused on analyzing and/or designing candidate PEBB converter topologies and associated switching control strategies that permit zero-current switching of the MCTs (or IGBTs). This zero-current switching is expected to reduce turn-off losses associated with the inherent tail currents of these MOS-gated bipolar devices. As with zero-voltage switching in the ARCP topology, zero-current switching is generally effected through the use of an auxiliary switched resonant tank. Various converters differ in the circuit topology of the switches and resonant components and in the timing control of the main and auxiliary switching.

An analysis process has been applied to four candidate converter topologies and associated switching control strategies, to illuminate trade-offs among semiconductor and passive component stress, operating limitations, and control complexity. There are four steps in this analysis process leading to a detailed simulation of a candidate converter. These four steps are:

1. Analysis assuming ideal component models.
2. Concept simulation in Saber® using static timing and simplified component models.
3. Control synthesis.
4. Detailed waveform simulation in Saber using dynamic timing and advanced models for the MCTs and resonant components.

In addition to providing a detailed, parameterized simulation for design purposes, this procedure yields valuable insights into the operation and stability of the topology/strategy.

Some candidate topologies/strategies have been provided by NSWCCD/P, while others have been derived at PSU from original concepts or the literature. Four candidates that have been considered can be described briefly as follows:

- A resonant bridge topology and two-switch control strategy that provides zero-current turn off as well as zero-current turn on of all MCTs but requires a moderately complex controller.
- A resonant bridge topology, which is essentially equivalent to the McMurray thyristor commutating circuit. This design provides zero-current turn off but full-load current turn on using a simple controller. There is, however, a significant trapped energy problem inherited from the McMurray circuit.
- A resonant bridge topology and two-switch control strategy that provides zero-current turn off but full-load current turn on with a relatively simple controller and without a trapped energy problem.
- An ARCP-like topology that provides zero-current turn off and adjustable-current turn on but requires a moderately complex controller.

Each topology/strategy is described in a self-contained chapter that begins with a basic description and an overall assessment. In each case, this is followed by a progressively more detailed analysis and description of basic controller requirements.

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CHAPTER 1
INTRODUCTION

It has been suggested that to overcome the significant turn-off current tails common to minority carrier devices, future PEBB designs utilize a converter topology and associated switching control strategy that provide zero-current switching. This represents a departure from the PEBB 1, in which an ARCP topology was used to provide zero-voltage switching. As in the ARCP, however, an auxiliary-switched resonant circuit is used in most zero-current switching topologies to effect low-loss commutation of the main pole switches. Specific converter topologies differ in the interconnection of the auxiliary switches and resonant components.

Associated with each converter topology is a switching control strategy that must coordinate the gating signals for the main and auxiliary switches so as to obtain a resonant circuit response that provides opportunities for zero-current switching. In this context, the switching control strategy represents the closest-to-MCT and highest bandwidth portion of a control hierarchy that typically includes PWM signal generation and an application controller. This control hierarchy is illustrated in Fig. 1.1 for a three-phase motor drive application. Often, the need for close interaction (minimum propagation delays and /or feedback) between the switching controller and the converter necessitates that the switching controller be implemented in high-speed digital and/or analog hardware that can be connected directly to the gate drives of the converter switches. In this case, the switching controller may receive signals from a standard PWM signal source, such as a space vector modulator that is implemented using a digital signal processor (DSP) or microcontroller (μC). Because standard PWM signals are generated only for the main switches, the switching controller must accept these as requests and generate gating signals for the auxiliary switches as well as the actual gating signals for the main switches. An alternative approach is to combine the role of the PWM signal generator and switching controller within a single DSP or μC. This approach eliminates

a fair amount of hardware, but requires a very fast DSP or μC, which may also have to have high-bandwidth analog inputs.

A wide variety of zero-current switching topologies/strategies can be considered for the PEBB 2. Many of these topologies/strategies were developed years ago as commutating schemes for conventional thyristors in high-power dc-to-dc and dc-to-ac converters [1]. Additional topologies have been proposed more recently for use with IGBTs and MCTs [2,3]. The large number of approaches is indicative of the need to optimize topologies around specific characteristics of different (sub) classes of power devices and around application requirements. With the introduction of the new MCT technology, it is again desirable to re-examine existing approaches and to consider the new unique requirements and features of these devices. There is also a pressing need to consider the particular volume, weight, and reliability requirements of Navy applications.

Assessment of four different topologies and strategies is currently underway using a flexible and well reasoned analysis process. This process is intended to illuminate trade-offs among semiconductor and passive component stress, operating limitations, control complexity, and application-specific performance. For each topology/strategy in which these trade-offs appear to be promising, a detailed simulation that can be used as an aid in final circuit design is to be produced.

The assessment process is described in the following section, which begins with a relatively brief overview of the process and its constituent steps. Each of these steps is then described in greater detail in its own subsection for the interested reader. The overview by itself should be sufficient for a reader to proceed to Section 1.2 wherein results from the analysis of four candidate topologies/strategies are summarized. More detailed information about each topology/strategy is provided in a subsequent chapter.

1.1 Assessment Process

Assessment of each candidate converter topology and switching control strategy for the PEBB 2 is being conducted using established analytical techniques. The process of applying these techniques is illustrated in Fig. 1.2, which shows a complete analysis and design cycle. As a starting point for the analysis and design process, waveforms for key converter variables are derived based on an assumption of ideal component models. This analysis provides valuable insight into converter operation and facilitates derivation

of mathematical expressions for operating limits and design optimization. The idealized waveforms are also useful when determining gating control signals to be used during concept simulation, the second step shown in Fig. 1.2.

A concept simulation for each topology/strategy is performed using Saber® [4]. The purpose of this simulation is to verify the idealized analysis and to introduce some second-order effects such as diode reverse recovery and the finite "Q" of the resonant circuit. At this step in the process, the simulation is not a true design aid, because switching gating signals are programmed statically and easy-to-use IGBT models rather then more accurate but cantankerous MCT models are used for the switches. Once the basic concept has been verified, gating control synthesis and refinement of the simulation to include greater detail can proceed in parallel.

The starting point for control synthesis is the selection off a basic approach from a spectrum that ranges from pure relative-time schemes to state-feedback methods. Generally, relative-time control, in which gating signals are generated based upon the expected response of the converter, is the simplest but least robust. State feedback, on the other hand, can be made robust to a variety of parameter and operating condition changes but may have significant sensor and/or processing requirements. Hybrid approaches, which combine aspects of both relative-time and state-feedback, can and probably should be used for the PEBB 2. An important part of control synthesis is the identification of timing delays in the software, gate drive circuits, and possibly the sensing circuits.

Concurrent with controller synthesis, the concept simulation can be enhanced to provide design support by incorporating more accurate MCT models for the switches and third-order effects in the resonant components. Ultimately, models of the controller can also be incorporated with the more detailed converter simulation. The resulting simulation can then be used effectively as a design aid. This process has been used successfully to advance development of the Penn State ARCP [5].

More detailed information regarding each step in the analysis process is presented in the following subsections. A summary of analysis results for our candidate topologies and switching control strategies is presented in the next section. A complete analysis for each topology/strategy is presented in one of the subsequent chapters.

Waveform Analysis

The first step in analyzing the performance of a candidate topology and associated switching strategy is to obtain the voltage and current waveforms of the resonant capacitor and inductor, respectively. For a topology/strategy from the literature, these waveforms can be derived readily from a description of the circuit and switching sequence. For a new design, the switching sequence is selected to produce a series of resonant pulses that together form a periodic response in which the timing of the rising and falling edges of the pole voltage can be controlled. It is convenient to think of each resonant pulse as an essentially discrete transition from one set of capacitor voltage and inductor current states to another, even though the transitions actually follow circular (continuous) trajectories in the so-called current-voltage state plane.[2] The term discrete is used here to describe the transitions, because from a given set of initial capacitor voltage and inductor current values there is generally a small finite set of final values that simultaneously satisfy the constraints of being approachable along a circular trajectory and being consistent with the on/off characteristics of the diodes and switches. Selection of each transition is, therefore, based on the utility of its end point as either a zero-current condition for switching or the starting point for a subsequent transition. Alternative sequences are compared using the maximum voltage and current excursions during resonant pulses as metrics because these excursions correspond to stress on the semiconductor devices and passive components. A second important metric is the timing of the rising and falling edges of the pole voltage relative to the initiation and/or completion of the resonant pulses. This relative time influences the simplicity/robustness of the hardware controller as well as the harmonic content of the output voltage and the utilization of dc input voltage.

In the analyses presented in subsequent chapters, circuit response during commutations from S1 to D2 (S1→D2) and from D2 to S1 (D2→S1) are the only ones that are considered, because complimentary commutations are symmetric. Moreover, to permit derivation of closed-form expressions for the response of each design, it is assumed that quasi-steady-state conditions prevail. In particular, it is assumed that the

[2] State-plane analysis provides an especially convenient graphical method for determining the circuit response. In particular, the aforementioned circular trajectories represent the exchange of energy between the capacitor and inductor ($\frac{1}{2}Cv^2 + \frac{1}{2}Li^2 = E_o$) during resonance with time used as a parameter. A primer on state-plane analysis is included in Appendix A for reference.

resonant capacitor is charged to a particular periodic steady-state voltage at the start of either or both commutations. A start-up sequence is shown explicitly for those designs in which requisite charging of the resonant capacitor does not occur automatically.

Once the response has been established graphically, it is verified via a concept simulation. It can then be used to determine mathematical relationships between peak values of variables or timing intervals. These relationships provide the basis for design optimization, sensitivity analysis, and harmonic assessment.

Concept Simulation

Simulations of a converter topology are conducted using Saber to verify the idealized analysis and to incorporate second-order effects. The switch signals in the simulation are generated using pulse voltage sources with fixed pulse widths and periods taken from the waveform analysis. The switches themselves are represented using IGBT models rather than the Harris-provided MCT models, because the MCT models are exceptionally detailed and hence slow to execute. At this point in the analysis/design cycle, simulation speed is more important than fine detail. Moreover, the static programming of the gating signals is inconsistent with studying detailed switching performance.

Although the IGBT models provide less accuracy than MCT models might, the IGBT models do provide an indication of the second-order effects associated with turn-off tail. Other second-order effects that can be modeled readily in the concept simulation include diode reverse recovery and the finite Q of the resonant circuit. Diode reverse recovery can have a significant influence on the circuit response beyond the usual impact on device ratings. For example, diode recovery can require that additional time be allowed for resonance as inductor currents carried by a diode are not blocked at zero but actually go negative. The resulting energy stored in the inductor must then be transferred to a capacitor (or the load) over time. Second and third-order effects related to the resonant circuit include self-resonance and parasitic resistance/conductance in each of the components. Except for the effect of resistance on Q, these are not significant in many of the designs, because it is expected that the components to be used in the actual implementation will be selected thoughtfully.

Control Synthesis

Control synthesis involves the design of hardware and/or software to transform user-provided PWM signals for the upper and lower main pole switches and for the auxiliary switches. Generally, commutation is initiated by gating one of the auxiliary switches to start a resonant pulse; gating of a main switch follows gating of the auxiliary switch at (near) the instant in the resonant pulse where the resonant inductor current equals the output current. Three general categories of gating control can be used to realize this sequence: (1) relative-time control, (2) state-dependent (feedback) control, and (3) hybrid relative-time/state-dependent control. Relative-time control is based on the expected resonant circuit response, which includes some degree of uncertainty both in terms of parameter values and unmodeled dynamics. If bounds on the uncertainties in the response can be determined, relative-time control eliminates the need for additional sensor hardware thereby reducing component/packaging costs and increasing reliability. The lack of feedback, however, makes it difficult or impossible to accommodate fault or other unanticipated conditions.

State-dependent control relies on detecting specific instantaneous conditions within the circuit (e.g., the zero crossing of the MCT current as resonant current approaches and then exceeds the output current) in order to determine appropriate gating signals. This method leads necessarily to abundant feedback that can be used to accommodate parameter variation and/or fault conditions but occupies volume and introduces reliability/interference issues. Moreover, delays inherent in the sensor hardware and detection scheme can introduce complications.

A hybrid approach can reduce the feedback requirements to those states that can be used to predict easily and accurately relative-time control actions. For example, in one of the candidate designs the gating signal to turn off a main switch should follow the gating signal to turn on the auxiliary switch by approximately three-quarters of a resonant period. In a pure relative-time control the timing difference in the signals would be set based on the nominal L and C values. Variation in the as-built component values can be accommodated readily with a hybrid approach by determining the actual (half) period from detection of the resonant inductor zero-crossing that occurs halfway through the resonant cycle.

Detailed Simulation

A detailed simulation is produced to serve as an aid to the circuit designer. These simulations can be obtained from the concept simulation by substituting MCT models for IGBT models, providing more realistic behavioral models for the gate drives, and including parasitics in the main and auxiliary power circuits. Ideally, the model of a controller that is to be realized using digital and analog hardware can also be included in the simulation.

In order to provide useful design guidance, at least some parts of the simulation must be validated. A key aspect in this regard is switching performance of the MCTs, which is closely related to gate drive performance. Fortunately, both of these can be examined readily in the laboratory and used to "tune" the simulation without necessarily having to build a complete converter. Similarly, the frequency response of the resonant circuit can be measured readily by itself. Parasitics in the main and auxiliary power circuits are more difficult to measure/estimate, but are relatively minor.

This level of simulation provides an opportunity to study some aspects of the design more readily or even more accurately than is possible with actual hardware. For example, the effects of changes in the gate drive and/or resonant circuits on dissipation at turn on and turn off can be examined. Stability and short-circuit response can also be studied more safely than with actual hardware.

1.2 Preliminary Analysis Results of Four Candidate Converter Topologies and Associated Switching Control Strategies

Four different topologies/strategies have been considered to date. A name, origin, and brief description of each topology/strategy and its features are given in Table 1.1. A basic resonant bridge, which is used in three of these, is shown in Fig. 1.3 for reference. In this circuit, a resonant tank (L and C) spans the center points of two poles. The main pole is comprised of S1, S2, and their anti-parallel diodes, while a second auxiliary pole is comprised of S3, S4, and anti-parallel diodes.

Based on the work to date, advantages (+), disadvantages (–), and points of interest (·) have been identified for each topology/strategy. These are summarized here. More detailed information is provided in subsequent chapters – one chapter per topology/strategy.

Table 1.1 List of converter topologies and switching control strategies.

Designator	Origin	Description/Features
MLZDCB	Virginia Power Electronics Center [1] (Mao, Lee, Zhou, Dai, Cosan, Boroyevich)	Resonant bridge circuit. Zero-current switching at turn-on and turn-off of all switches.
BRDCY	CDNSWC/A Code 813 (Borraccini, Rudy, Duong, Cochran, Yuen)	Resonant bridge circuit with blocking diodes in series with auxiliary switches (essentially the classic McMurray thyristor commutating circuit). Zero-current turn-off of all switches.
SSM	Penn State University (Shorter, Salberta, Mayer)	Resonant bridge circuit. Zero-current turn-off of all switches.
ACSMM	McMurray	AC-Switched Modified McMurray

The MLZDCB Topology/Strategy

This is a true zero-current transition topology/strategy, in which all controlled switches are turned on and turned off under zero-current [3].

+ Zero-current turn on as well as zero-current turn off

– Long "turn-around time"[2] of approximately 2.75 times the resonant period. This will adversely effect dc bus voltage utilization and total harmonic distortion.

· Control requirements are moderately complex, but a relatively simple yet robust hybrid approach is possible provided a precision timer controlled via feedback could be utilized.

[2] Turn-around time is defined here as the total time required to complete both an S1→D2 and D2→S1 commutation. This time includes all resonant pulses and constant current or voltage intervals. It is assumed that this time is essentially unavailable for applying controllable volt-seconds to the load.

The BRDCY Topology/Strategy

This topology is designed to eliminate the long turn-around time of the MLZDCB by utilizing blocking diodes in series with the auxiliary switches to prevent "extraneous" resonant (half) cycles. Addition of these diodes yields what is essentially the classic McMurray thyristor commutating circuit.

+ Nearly minimum turn-around time with simple relative-time control.
– Trapped energy problem inherited from McMurray.
– Full-load turn on of the MCT will overstress the opposite, off-going diode.
· One-sided resonant inductor current pulses may lead to noise problems.

The SSM Topology/Strategy

This is another "pure" resonant bridge topology like the MLZDCB; however, zero-current turn on has been sacrificed to reduce turn-around time.

+ Moderate turn-around time of approximately 2 times the resonant period.
. Control requirements are between simple and complex; a relative-time control can be used, because turn off of a main switch occurs less than a quarter of a resonant period after gating an auxiliary switch.
– Full-load turn on of the MCT may overstress the opposite, off-going diode.

The ACSMM Topology/Strategy

This is an ARCP-like topology in which the snubber (resonant) capacitors are moved to the position occupied by the bank capacitors, which are omitted.

+ ARCP-like topology permits use of existing packaging.
+ Adjustable turn-on current can be used to reduce diode stress.
– Long turn-around time of approximately 3 times the resonant period.
– Commutating current pulse flows through the main switch. This can be accommodated by the MCT but counts against thermal margin.

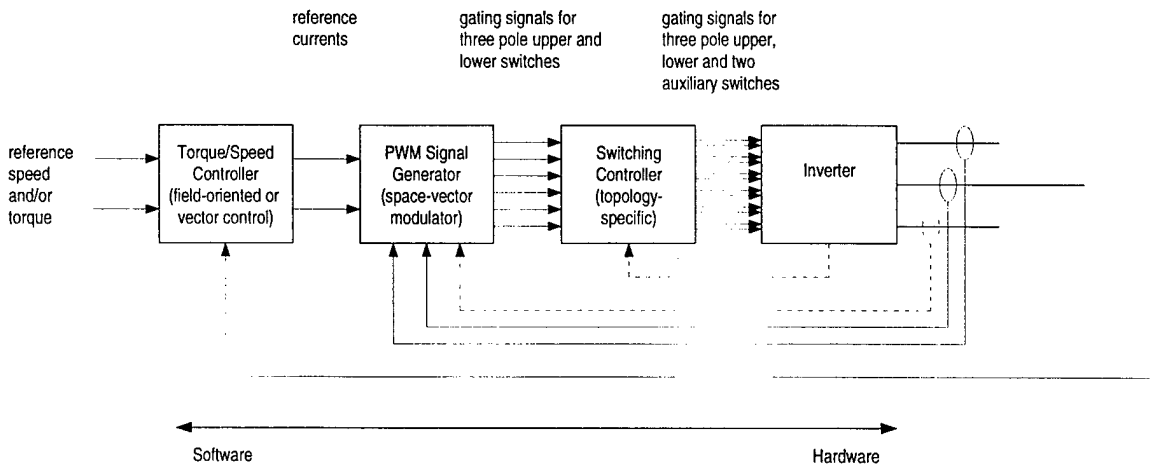

Figure 1.1. Block diagram showing control hierarchy in a motor drive application.

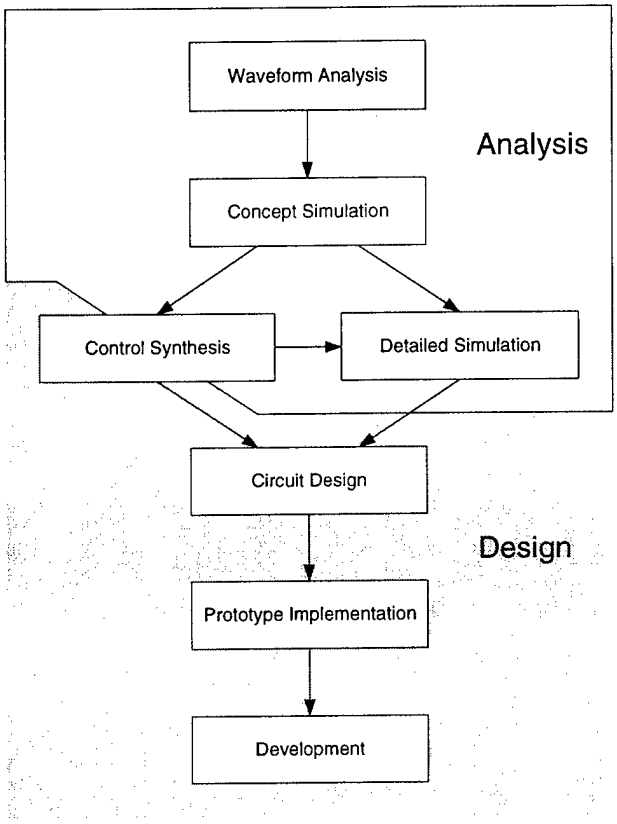

Figure 1.2. Analysis and design process.

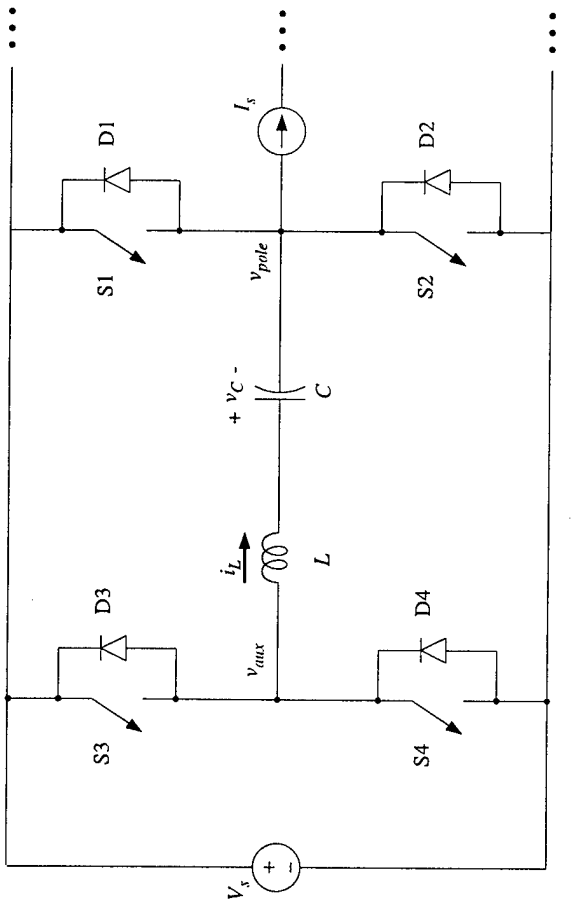

Figure 1.3 Basic resonant bridge circuit.

CHAPTER 2
RESONANT BRIDGE WITH ZERO-CURRENT TURN-OFF AND ZERO-CURRENT TURN-ON

2.1 INTRODUCTION

In this chapter, a converter topology and switching control strategy that provide both zero-current turn off and zero-current turn on of all switches [3] are described. The topology is a resonant bridge that can be assembled readily from two-phase switches as shown in Fig. 2.1. The advantage of both zero-current turn on and turn off is countered somewhat by significant turn-around time and the related problem of moderately complex control.

A turn-around time of approximately 2.75 times the resonant period ($2.75T_0$) is dominated by a ¾-cycle swing between initiation of each commutation and the resulting voltage transition. Each transition is then followed by an interval of either essentially constant inductor current or capacitor voltage and another ¼-cycle swing. The significant delay of $¾T_0$ between initiation of commutation and the actual turn on/off of the main switch leaves the design susceptible to problems arising from controller/drive timing delays or uncertainties in the resonant circuit response. These can be overcome but will likely preclude a simple relative-time control. Moreover, the long turn-around time limits (severely) the range of allowable duty cycles. This can impact application-specific performance by either precluding low total harmonic distortion (THD) output and/or requiring sophisticated PWM signal generation.

2.2 WAVEFORM ANALYSIS

The capacitor voltage v_C, inductor current i_L, pole voltage v_{pole}, and auxiliary voltage v_{aux} waveforms along with the switch gating signals are shown in Figs. 2.2 and 2.3. As indicated in these figures, which represent the D2→S1 and S1→D2 commutations, there are 15 instances of interest during each PWM cycle: t_0 through t_{10} correspond to those defined in [3], while t_{S4off1}, t_{S1on}, t_{S4off2}, and t_{S1off} are defined in the

figure. The event and/or control action that occurs at each instant are described in this section.

t_0: Initiation of D2→S1 commutation

The process of commutating the output current I_s from D2 to S1 to begin a new PWM cycle commences at t_0 with the gating on of S4 to produce a resonant inductor current pulse i_L, which is initially negative, as the resonant components are in a loop with S4 and D2, and the capacitor voltage is positive. It should be noted that the subsequent pole voltage transition actually occurs approximately three-quarters of a resonant cycle later at t_2.

t_1: Natural S4→D4 commutation

A natural commutation of i_L from S4 to D4 occurs at t_1 as i_L crosses zero going positive.

t_{S4off1}: First controlled zero-current turn off of S4

Once the current through S4 is zero, this switch can be turned off with minimal stress.

t_2: Instant of maximum i_L or minimum i_{S1}

The maximum of i_L occurs at t_2, which is $\frac{3}{4}T_0$ after t_0. Ideally, i_L would equal I_s at this instant, so by Kirchoff's current law, the current through D2 would be zero.

t_{S1on}: Controlled zero-current turn on of S1

Switch S1 should be turned on as close to t_2 as possible to minimize turn-on stress for S1 and to avoid excessive *di/dt* on D2.

t_3: Zero crossing of i_L

Following turn on of S1 at t_{S1on}, i_L is driven toward zero along the trajectory determined by the voltage difference between v_{aux} (one diode drop below ground) and v_{pole} (rail voltage minus voltage drop across S1). Ideally, i_L would be driven to zero but not below, due to D4.

t_{3a}: Reverse recovery time of D4

Diode D4 does not turn off ideally at zero current. Instead it draws a reverse recovery current, which allows i_L to go to a negative value corresponding to the I_{rr} rating of the device. Once the diode fully recovers, the energy in the inductor ($\frac{1}{2}LI_{rr}^2$) is transferred to the capacitor resonantly.

t_4: Completion of D2→S1 commutation

The commutation from D2 to S1 is completed once the D4 reverse recovery energy trapped in the resonant inductor at t_{3a} has been transferred to the capacitor.

t_5: Initiation of S1→D2 commutation

The process of commutating I_s from S1 to D2 commences at t_5 with the gating on of S4 to produce a resonant current pulse i_L, which is initially negative as the resonant components are in a loop with S4, the dc voltage source V_s, and S1. It should be noted that the subsequent change in pole voltage actually occurs approximately ¾ of a resonant cycle later at t_8.

t_6: Natural S4→D4 commutation

A natural commutation of i_L from S4 to D4 occurs at t_6 as i_L crosses zero going positive.

t_{S4off2}: Second controlled zero-current turn off of S4

With $i_L > 0$, the current through S4 is zero and S4 can be turned off without stress.

t_7: Natural S1→D1 commutation

A natural commutation from S1 to D1 occurs at t_7 as i_L exceeds I_s. By Kirchoff's current law, i_{S1} would otherwise be forced negative.

t_{S1off}: Controlled zero-current turn on of S1

Switch S1 should be turned off as soon as possible after t_7 to ensure that it has adequate forward blocking voltage capability at t_8 when its anti-parallel diode D1 begins to reverse bias.

t_8: Natural turn off of D1

Diode D1 turns off naturally at t_8 as i_L drops below I_s. (In simulations and the actual circuit, the difference i_L - I_s goes significantly negative due to reverse recovery of the diode.)

t_9: Natural commutation of I_s to D2

Once the capacitor voltage has been driven to zero by the constant current drawn by the load, the voltage at the pole node reaches zero and D2 becomes forward biased. Subsequently, D2 begins to pick up I_s as the trapped inductor energy is transferred to the capacitor.

t_{10}: Completion of S1→D2 commutation

Once i_L reaches zero (i.e., the trapped inductor energy has been fully transferred to the capacitor), D4 reverse biases and turns off naturally.

The analysis presented here is referred to again in Section 2.4 where control synthesis is described.

2.3 CONCEPT SIMULATION

Concept simulations of this topology and strategy have been performed to validate the previous analysis and to provide a basis for more detailed simulations to be used in design. A schematic of the circuit entered in Saber is shown in Fig. 2.4. Each switch in this simulation is modeled as an IRGPC50F IGBT, which has voltage and current ratings of 600 V and 280 A, respectively. The tail interval is programmed to be approximately 270 ns, which is similar to the tail interval observed in the MCT models provided by Harris. The diode is modeled as an ESM 244_600, which has voltage and current ratings of 600 V and 800 A, respectively. This diode is particularly useful due to its relatively rapid reverse recovery characteristics and reverse recovery current limit of 6 A, which are representative of diodes that are likely to be used in an implementation. The voltage source and current source are simple dc sources without ac noise. The capacitors and inductors are also basic devices with initial conditions set to zero. All resistor components are set to the indicated values without thermal effects being simulated.

The converter was simulated under a variety of load conditions ranging from I_s = 20 A to I_s = 150 A. Operation at I_s = 50 is depicted in Fig. 2.5, which shows the auxiliary voltage v_{aux}, the pole voltage v_{pole}, the resonant inductor current i_L, the resonant capacitor voltage v_C, the upper main switch current i_{S1}, the lower auxiliary switch current i_{S4}, and the corresponding switch gating signals. To facilitate comparison between these simulation waveforms and the previous analysis, the simulation time of several of the key instants are listed in Table 2.1. The overall similarity between these waveforms and those in Figs. 2.2 and 2.3 indicates that the analysis is correct. The only noticeable differences occur at 456 μs (t_1), 459 μs (t_3) 480 μs (t_7), and 489 μs (t_{10}). The slight variations at 456 μs and 480 μs are associated with ringing as S4 turns off. Similarly, at 459 μs and 489 μs there is ringing as D4 turns off.

Table 2.1 Comparison of Analysis and Simulation Times

Analysis Instant	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
Simulation Time (μs)	450	456	458	459	461	475	480	482	483	485	489

2.4 CONTROL SYNTHESIS

Control synthesis for the MLZDCB centers on ensuring that t_{S1on} and t_{S1off} occur as close as possible to t_2 and t_7, respectively. The turn off at t_{S1off} is probably more critical due to the potentially significant circuit-commutated turn-off time t_q associated with the MCT. For that reason, discussion will focus on the hardware/software requirements to control that transition; most or all of the results can be applied directly to controlling t_{S1on}.

The presence of nearly three-quarters of a resonant cycle between the controlled initiation of the S1→D2 commutation at t_5 and start of the safe turn-off interval for S1 at t_7 makes a pure relative-time scheme somewhat unattractive. In particular, small variations between design and as-built values for the resonant components and/or operating variations in these components or the Q of the resonant circuit may lead to incorrect timing. Instead, a relative-time control that is with respect to t_6, which is relatively easy to detect, provides a significantly more robust design while still being fairly simple. Three different methods for relative-time control with respect to t_6 are discussed here. Each method represents a different degree of trade-off between conservatism in accommodating t_q and simplicity of hardware.

In theory, the earliest possible time for t_{S1off} is t_7 and could be calculated relative to t_6 using an expression for the resonant circuit response. In particular,

$$t_7 = t_6 + \sin^{-1}\left(\frac{I_s}{\sqrt{\frac{C}{L}}(V_s - \Delta_2 V_C)}\right) \qquad 2.4\text{-}1$$

where V_s and I_s could be measured (i.e., as in a feedforward control), C and L would be assumed to be near their design or as-tested values, and $\Delta_2 V_C$ would correspond to the D4 reverse recovery energy stored at the end of the previous D2→S1 commutation – this could likely be neglected. The value of t_6 used in the calculation would be obtained by

subtracting from a measured zero-crossing time the estimated propagation delay associated with the current zero-crossing detector hardware and processing delays in a DSP/digital controller. Utilizing this information, and predicting when the resonant current exceeds I_s, it is possible to switch S1 off optimally. By gating off S1 shortly after the resonant current exceeds I_s, the switch will have the maximum time to turn off.

A second approach that eliminates reliance on establishing the resonant component parameter values but is less optimal in terms of providing maximum turn-off time to accommodate t_q, is to approximate the sine function between t_6 and t_7 with a linear ramp starting at zero at t_6 and increasing with a slope of $I_{L,peak}/(¼T_o)$. Both of these parameters are readily available if the i_L waveform (not simply its zero crossing) is available to the DSP (i.e., a feedback control). The intersection of this ramp with the (nearly constant) measured I_s would necessarily lie between t_6 and $t_6 + ¼T_o$. A significant concern with this approach is accurate detection of the peak current, as the sensor hardware would have to have a large dynamic range.

A third approach would be to use a constant time of one-quarter resonant period following the derived t_6. This would eliminate the need both for parameter values and $I_{L,peak}$, by always timing turn off of S1 at $t_6 + ¼T_o$. This has the advantage of simplicity but comes at the expense of reducing the margin on turn off time for S1.

For the last two methods, it is necessary to have some information regarding the instantaneous value of i_L (or at least its zero-crossing time) be available to the DSP and control algorithm. There are several methods for sensing this current including:

1. LEM current sensor.
2. Sense resistor, differential amplifier, and isolation amplifier
3. Sense resistor, differential amplifier, and instrumentation amplifier.
4. Sense resistor, differential amplifier, and optocoupler (only indicates zero crossing).
5. Hardware integrator for inductor voltage.
6. Software integrator for inductor voltage.

Basic characteristics and design considerations for several of these methods are described in Appendix B.

2.5 Design Optimization and Trade-Offs

In the analysis described in Section 2.2, specific values for the resonant inductor L and capacitor C were not necessary, as a normalized state-plane was employed. In the design of a practical converter, however, the selection of L and C is critically important to obtain "optimal" converter performance and avoid excessive component stress. The selection of L and C is done best by a process in which "optimal" converter performance is defined explicitly (mathematically). Such a process is described in [Mao96] and is repeated here with some modification/corrections and annotation.

Ultimately, the process of selecting L and C will require identifying the maximum dc input voltage V_s and the maximum (instantaneous) ac output current I_s specifications for the converter as well as the circuit-commutated turn-off time t_q of the main and auxiliary switches. These values then represent design parameters. Within the process, it is assumed that there are two primary criteria for optimal performance of the converter. The first is related to t_q of the main switches. In particular, the window in which to turn off S1 under zero current must be greater than t_q by up to a factor of two, depending upon the gating control method (see previous section). This criterion is necessary to avoid inadvertent turn on of a main switch, and it will lead to a mathematical relationship between the resonant period T_o, which is related to L and C, ($T_0=2\pi(LC)^{1/2}$), and the ratio of the output current I_s, to the peak resonant inductor current $I_{L,peak}$; this ratio is a key design variable and will be referred to as m. The second criterion is that the additional conduction losses in the auxiliary and main switches due to the resonant current pulses should be minimal. This criterion will be met explicitly by minimizing a mathematical expression for the additional losses with respect to the design variable $m = I_s/I_{L,peak}$. The design process will now be described.

The starting point is determining the relationship between T_o and $m = I_s/I_{L,peak}$, given the constraint $T_{S1off} = t_8 - t_7 \geq t_q$. The boundaries of the T_{S1off} window are the intersections of the constant output current with the resonant inductor current pulse. These intersections can be expressed

$$I_s = I_{L,peak} \cos\left(\frac{2\pi t}{T_o}\right) \qquad 2.5\text{-}1$$

where it is assumed that the time reference is midway between t_7 and t_8. Solving for t

$$t = \frac{T_o}{2\pi}\cos^{-1}\left(\frac{I_s}{I_{L,peak}}\right) \qquad 2.5\text{-}2$$

This implies that

$$T_{off} = t_8 - t_7 = \frac{T_o}{\pi}\cos^{-1}\left(\frac{I_s}{I_{L,peak}}\right) \qquad 2.5\text{-}3$$

Denoting the ratio of I_s to $I_{L,peak}$ as m

$$T_{off} = \frac{T_o}{\pi}\cos^{-1}(m) \qquad 2.5\text{-}4$$

Ultimately, T_{off} will be set based on the design parameter t_q and m will be selected through an optimization (minimization) process, so this equation will provide the desired resonant frequency that, in turn, will provide L and C.

Although the resonant circuit is used to reduce switching losses of the pole switches, its resonant current pulses will result in new losses in the auxiliary circuit and greater conduction losses in the main switches. Intuitively, the magnitude of the additional losses will be related to the magnitude of the resonant current pulses, which can be expressed in terms of the design parameter I_s and design variable m (i.e., I_s/m). The exact expression for the additional losses can be derived in two parts. First the new losses will be expressed for the auxiliary circuit, which includes an auxiliary switch (corresponding to either the controlled device or the diode), the resonant inductor, and resonant capacitor. Second, the conduction losses in excess of the "hard-switched" conduction losses of the main switches will be expressed. In both cases, it assumed that the conduction losses can be expressed as the product of a constant voltage drop times an appropriate current. This constant-voltage model is much simpler to work with than a more realistic one that includes a constant on-state voltage for the switch plus an ohmic term Ri_L for the passive components. More accurate modeling is probably done better using a circuit simulation program. In any event, the auxiliary circuit voltage drop will be denoted V_c. The drop for the main switches will be denoted as V_c/k, where k typically lies between 2 and 4, as the "equivalent power" loss in the auxiliary circuit passive components corresponds to between ½ and ¾ of the auxiliary circuit losses.

The auxiliary circuit losses can now be expressed

$$E_{aux} = \int_{t_0}^{t_4} V_c |i_L| dt + \int_{t_5}^{t_{10}} V_c |i_L| dt$$

$$= V_c \left[\int_{t_0}^{t_1} -i_L dt + \int_{t_1}^{t_3} i_L dt + \int_{t_3}^{t_4} -i_L dt + \int_{t_5}^{t_6} -i_L dt + \int_{t_6}^{t_{10}} i_L dt \right] \qquad 2.5\text{-}5$$

Because i_L flows through the resonant capacitor, the various integrals of i_L in this expression can be related to the capacitor voltages at the bounds of integration.

$$E_{aux} = V_c C[-v_C(t_1) + v_C(t_0) + v_C(t_3) - v_C(t_1) - v_C(t_4) + v_C(t_3) - v_C(t_6) + v_C(t_5) + v_C(t_{10}) - v_C(t_6)] \qquad 2.5\text{-}7$$

This expression can be simplified by noting that $v_C(t_1) = -v_C(t_{10})$, $v_C(t_4) = v_C(t_5)$, and $v_C(t_3)$ is nearly zero.

$$E_{aux} = V_c C[4v_C(t_{10}) - 2v_C(t_6)] \qquad 2.5\text{-}8$$

To get back to an expression in terms of currents, note that $V_c(t_{10})$ is related to the energy in the capacitor at t_{10} and this energy is equal to the energy in the inductor at t_9

$$\tfrac{1}{2} C[v_c(t_{10})]^2 = \tfrac{1}{2} L[i_L(t_9)]^2 = \tfrac{1}{2} L I_s^{\,2} \qquad 2.5\text{-}9$$

Consequently, $v_C(t_{10}) = (L/C)^{1/2} I_s = (L/C)^{1/2} m I_{L,peak}$. The substitution for $v_C(t_6)$ is slightly more complicated. Assuming $v_C(t_4)$ is essentially zero (i.e., the diode reverse recovery energy stored in the resonant inductor is actually much smaller than indicated in Figs. 2.2 and 2.3), $v_C(t_6)$ lies at the leftmost point of a circle of radius V_s centered at the point (0,–V_s) in Fig. 2.3. From geometry, the energy at that point is exactly twice the energy at a point on the circular trajectory midway between t_5 and t_6 where i_L reaches its peak value of $I_{L,peak}$ (i.e., the length of a chord spanning 90° of a circle is $\sqrt{2}$ times the radius). Thus,

$$\tfrac{1}{2} C(2V_s)^2 = 2\left(\tfrac{1}{2} L I_{L,peak}^{\,2} + \tfrac{1}{2} C V_s^{\,2}\right) \qquad 2.5\text{-}10$$

so

$$V_s = \sqrt{\frac{L}{C}} I_{L,peak} \qquad 2.5\text{-}11$$

and

$$2v_C(t_6) = 2(2V_s) = 4\sqrt{\frac{L}{C}} I_{L,peak} \qquad 2.5\text{-}12$$

The losses in the auxiliary circuit can now be written

$$E_{aux} = V_c C\left(4\sqrt{\frac{L}{C}} m I_{L,peak} + 4\sqrt{\frac{L}{C}} I_{L,peak}\right) \qquad 2.5\text{-}13$$

$$= 4\sqrt{LC} V_c (1+m) I_{L,peak} \qquad 2.5\text{-}14$$

$$= 4\frac{T_0}{2\pi} V_c (1+m) I_{L,peak} \qquad 2.5\text{-}15$$

$$= \frac{2}{\pi}(1+m) T_0 V_c I_{L,peak} \qquad 2.5\text{-}16$$

The additional main switch losses occur when these devices carry resonant current with magnitude exceeding the magnitude of the output current. This occurs between t_7 and t_8 as well as in an interval lying between t_5 and t_6. For every other time during a resonant cycle, an increase (decrease) in main switch current is countered by a decrease (increase) at another time. The additional conduction losses in the main switches can be expressed

$$E_{main} = 2\int_{t_7}^{t_8} \frac{V_c}{k}\left[I_{L,peak}\cos\omega t - I_s\right] dt \qquad 2.5\text{-}17$$

$$= \frac{2V_c}{k}\left[\frac{1}{\omega} I_{L,peak}\sin\omega t\Big|_{t_7}^{t_8} - I_s t\Big|_{t_7}^{t_8}\right] \qquad 2.5\text{-}18$$

$$= 2\frac{V_c}{k}\left[\frac{T_0}{2\pi} I_{L,peak}(\sin\omega t_8 - \sin\omega t_7) - I_s(T_{off})\right] \qquad 2.5\text{-}19$$

$$= \frac{2V_c}{k}\left[\frac{T_0}{2\pi} I_{L,peak} 2\sqrt{1-m^2} - I_{L,peak} m\frac{T_0}{\pi}\cos^{-1} m\right] \qquad 2.5\text{-}20$$

$$= \frac{2V_c}{k}\left[\sqrt{1-m^2} - m\cos^{-1} m\right]\frac{T_0 I_{L,peak}}{\pi} \qquad 2.5\text{-}21$$

$$= \frac{2}{\pi}\left(\sqrt{1-m^2} - m\cos^{-1} m\right)\frac{V_c}{k} I_{L,peak} T_0 \qquad 2.5\text{-}22$$

The total additional losses due to the use of auxiliary resonant circuit can be expressed as the sum of the two separate components

$$E_{loss} = \frac{2}{\pi}\left[1 + m + \frac{\left(\sqrt{1-m^2} - m\cos^{-1} m\right)}{k}\right] T_0 V_c I_{L,peak} \qquad 2.5\text{-}23$$

Given V_s, I_s, T_{off}, and now V_c as design parameters, this expression can be normalized as

$$E_{normalized} = \frac{E_{loss}}{2V_c I_s T_{off}} \qquad 2.5\text{-}24$$

$$= \frac{1 + m + \left(\dfrac{\sqrt{1-m^2} - m\cos^{-1} m}{k}\right)}{m\cos^{-1} m} \qquad 2.5\text{-}24$$

This expression relates the additional losses due to the auxiliary circuit to the design variable m (and the design parameter k). A family of plots of $E_{normalized}$ vs. m is shown in Fig. 2.8 for k ranging from 1 to 5. From these plots, it can be deduced that the optimal value of m is in the interval [0.5,0.7]. The specific design value for m is denoted as M. Once M has been selected, the resonant period can be calculated after manipulating (2.5-4).

$$T_0 = \frac{\pi T_{off}}{\cos^{-1} M} \qquad 2.5\text{-}26$$

Because $T_0 = (LC)^{1/2}/2\pi$, there is now one equation relating the L and C parameter values that are being sought. A second equation comes from the relationship between $I_{L,peak}$ and V_s discussed previously. $I_{L,peak}$ in this equation can now be replaced by MI_s. The simultaneous solution of these two equations yields the following expressions for L and C

$$L = \frac{V_s T_{off}}{2MI_s \cos^{-1} M} \qquad 2.5\text{-}27$$

$$C = \frac{MT_{off} I_s}{2V_s \cos^{-1} M} \qquad 2.5\text{-}28$$

These formulas can be used to determine values for the resonant inductor and capacitor that can then be refined through simulation and/or experimentation.

The design optimization just described does not address the impact of turn-around time on converter performance, because the resonant period was determined based only on minimizing auxiliary circuit losses. To avoid the deleterious effects of turn-around time on bus utilization and THD, it may be necessary to accept additional losses.

2.6 Conclusions

Zero-current turn-on and turn-off make the MLZDCB an attractive candidate for future PEBB designs. The combination of long turn-around time and control complexity required to accommodate circuit-commutated turn-off time of the main MCTs or IGBTs, however, requires greater attention. A design process for selecting L and C given terminal variable magnitudes and basic device characteristics is available. This process will have to be extended and/or supplemented with simulation to obtain a design process or simulation model that includes the impact of turn-around time.

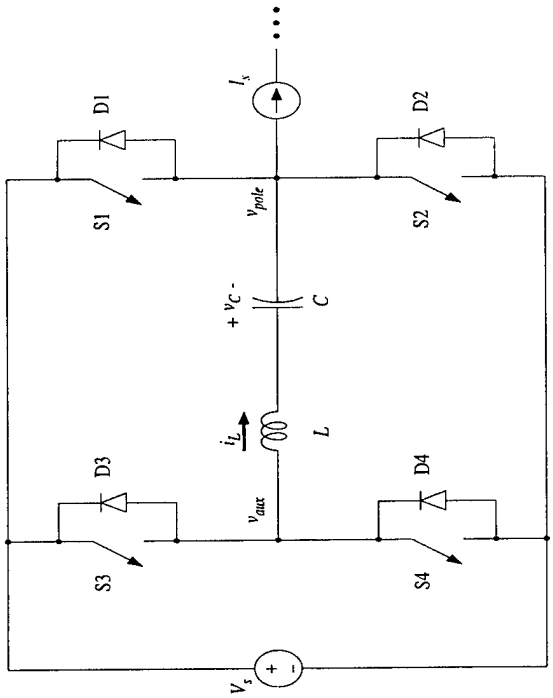

Figure 2.1 MLZDCB Basic Circuit

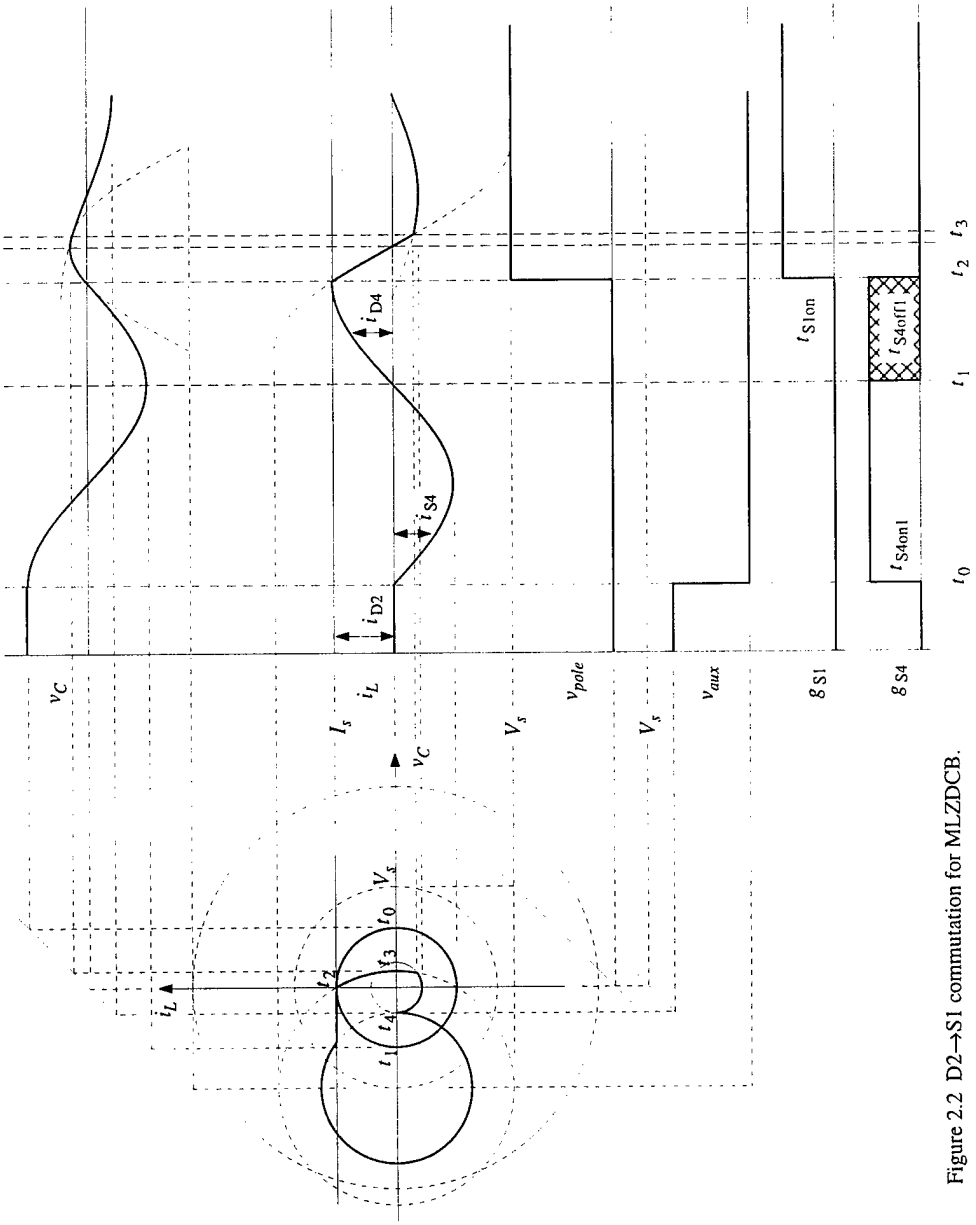

Figure 2.2 D2→S1 commutation for MLZDCB.

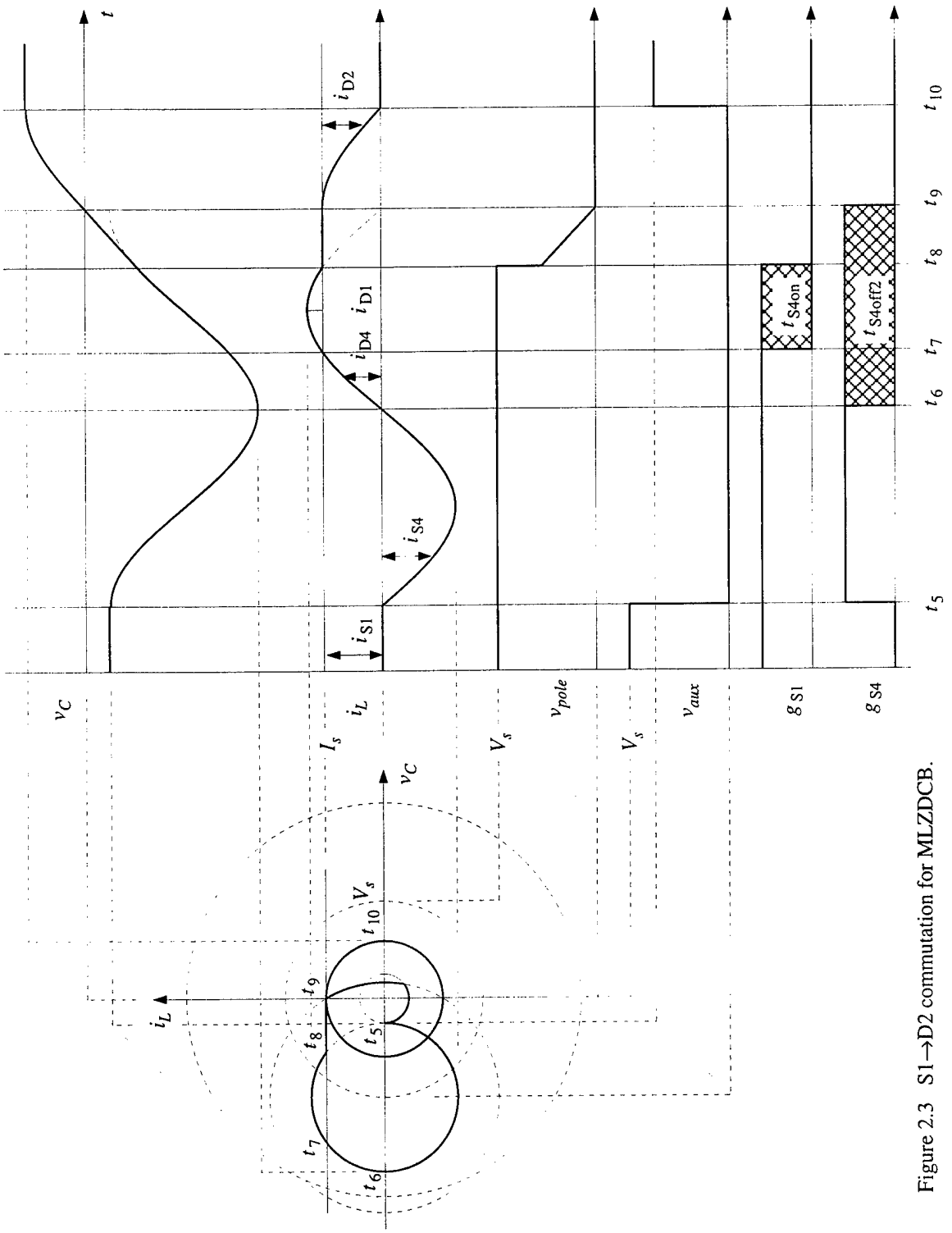

Figure 2.3 S1→D2 commutation for MLZDCB.

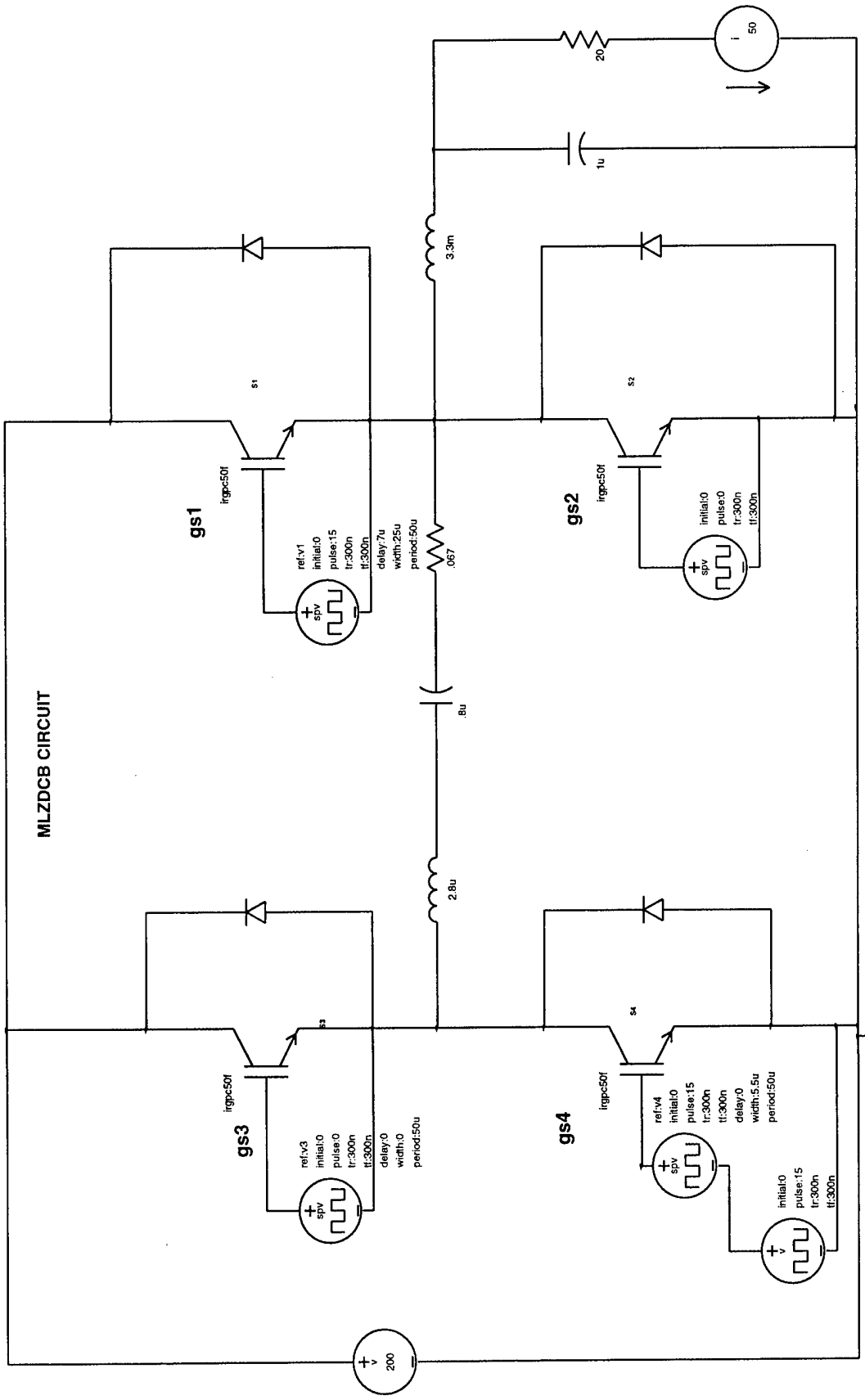

Figure 2.4 MLZDCB Circuit

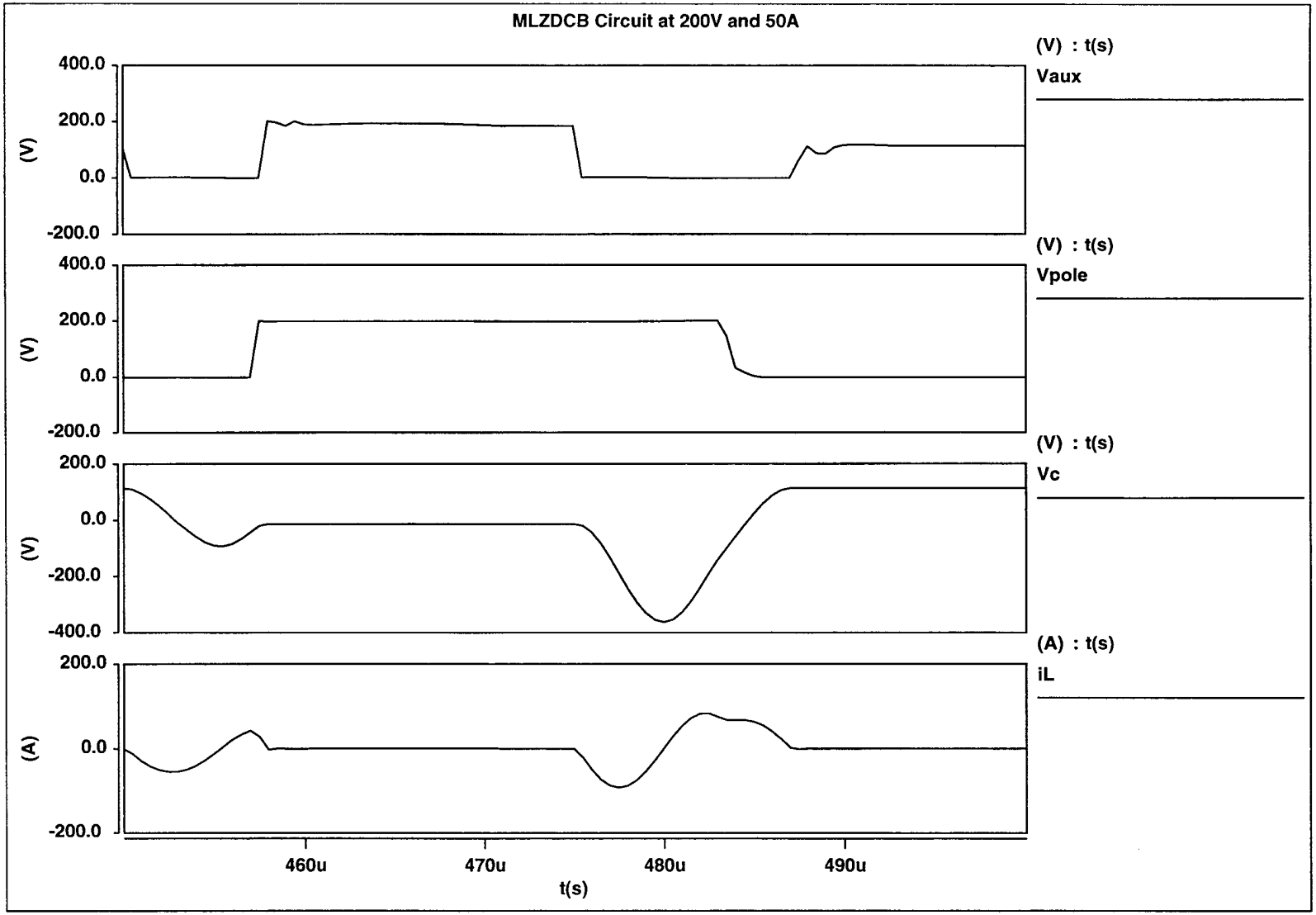

Figure 2.5 MLZDCB Circuit Resonant Waveforms

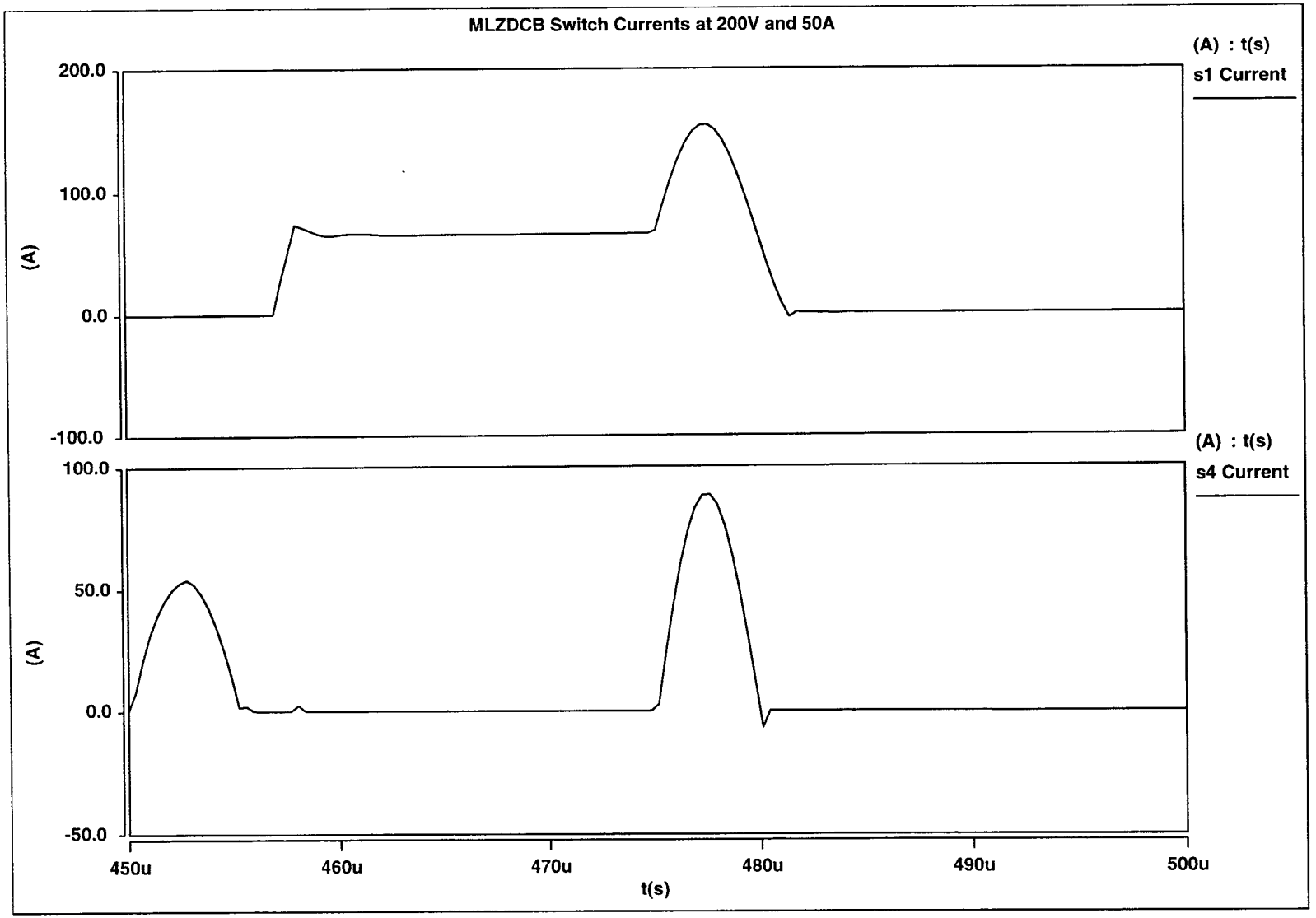

Figure 2.6 MLZDCB Switch Currents

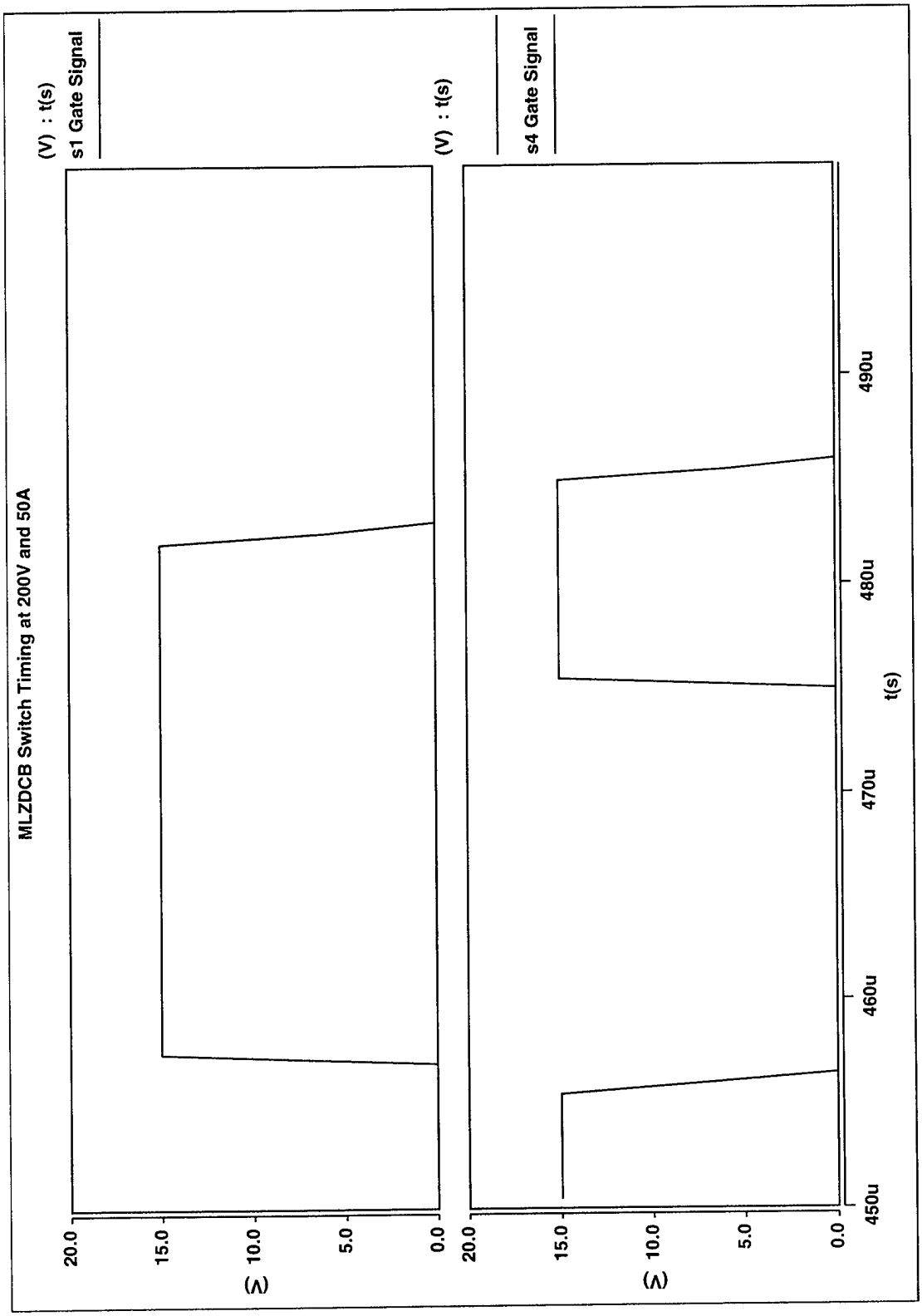

Figure 2.7 MLZDCB Switch Timing

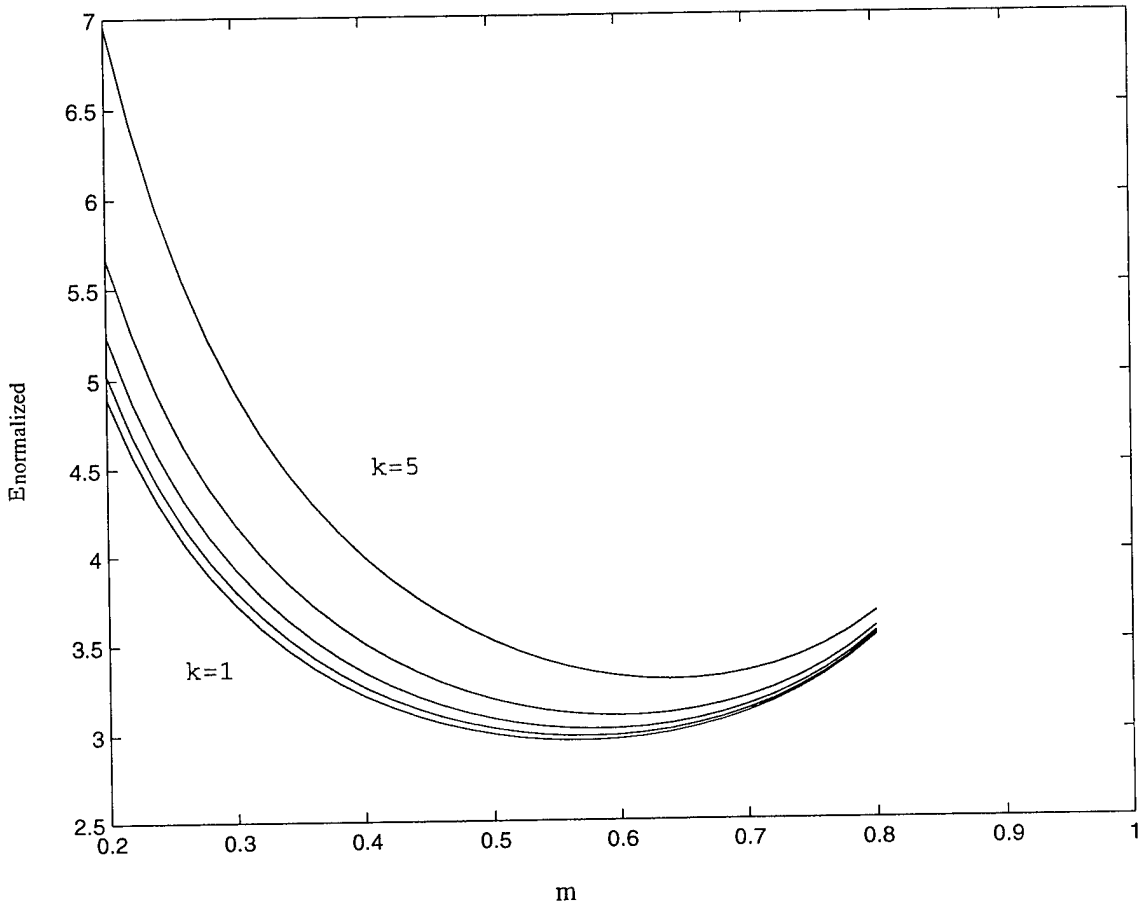

Figure 2.8 Plot of Enormalized vs. m

CHAPTER 3
RESONANT BRIDGE WITH BLOCKING DIODE TOPOLOGY AND ZERO-CURRENT TURN-OFF SWITCHING STRATEGY

3.1 INTRODUCTION

A resonant bridge with blocking diodes included in series with each of the auxiliary switches has been suggested as an alternative to the MLZDCB design described in Chapter 2. A schematic of this circuit is shown in Fig. 3.1. As in the MLZDCB or other resonant bridges, the resonant tank is connected between the center point of two poles or sets of phase switches. The main pole is the standard form, but the auxiliary pole includes blocking diodes D3b and D4b.

The purpose of the blocking diodes is to prevent reversals of the resonant inductor current as occurs in the MLZDCB. This reduces significantly the turn-around time associated with the MLZDCB. Unfortunately, addition of these blocking diodes results in what is essentially the classic McMurray thyristor commutating circuit. In particular, the blocking diodes obviate the free-wheel diodes in antiparallel with each of the auxiliary switches. Consequently, the auxiliary switches cannot be turned off under load due to the continuous current requirement imposed by the resonant inductor. Lacking turn-off-under-load capability, the auxiliary switches may just as well be thyristors.

As with the classic McMurray there is an energy build-up problem associated with this circuit. This can be seen readily in the state-plane/waveform analysis presented in the next section. Even without that analysis, a simple argument can be made to confirm the existence of the problem. In particular, instantaneous power flow – and therefore average power flow – out of the auxiliary node into the dc bus is impossible due to the blocking diodes. As long as the instantaneous power flow into the resonant tank through the auxiliary node is flowing out of the pole node, there will not be a build-up of energy in the resonant capacitor. At instances when an auxiliary switch and main switch are connected to the same rail, this is the case, because there is no net power into or out of the rail from or to the resonant tank. When opposite auxiliary and main switches are

on (e.g., S1 and S4), however, the resonant tank is in a loop with the dc voltage source, and energy is delivered to the resonant tank. The total energy in the resonant tank, which is stored in the capacitor at the end of each resonant cycle, increases with every cycle. This energy build-up is limited ultimately, as increased dissipation caused by larger resonant currents balances the incremental energy addition during each resonant cycle. Unfortunately, this balance could occur at relatively high capacitor voltages of several times V_s.

A second practical problem with this topology, at least for the first switching control strategy that has been considered, is the rapid turn on of a main MCT and its effect on the opposite diode. Specifically, the turn-on rate (*di/dt*) of the MCT actually exceeds the corresponding turn-off rate of most (all) diodes that can be used in this application.

Together the energy build-up in the resonant capacitor and the excessive *di/dt* make this topology a dubious choice for the PEBB 2.

3.2 WAVEFORM ANALYSIS

The capacitor voltage v_C, inductor current i_L, pole voltage v_{pole}, and auxiliary voltage v_{aux} waveforms along with the switch gating signals are shown in Figs. 3.2 and 3.3. As indicated in these figures, which represent the D2→S1 and S1→D2 commutations, there are eleven instances of interest during each PWM cycle. The event and/or control action that occurs at each instant are described in this section. An additional start-up sequence is required for this converter, as the state-plane trajectory never approaches the origin (i.e., a de-energized state). This additional sequence is described after the normal PWM sequence.

t_0: Initiation of capacitor voltage reversal

Prior to commutating the load current I_s from D2 to S1, it is necessary to reverse the resonant capacitor voltage v_C to the polarity required at the start of the subsequent S1 →D2 commutation. The voltage reversal is initiated by turning on S4 to form a loop comprised of the resonant capacitor and inductor as well as D4b, S4, and D2.

t_1: Completion of capacitor voltage reversal

The voltage reversal is completed a half-resonant period, $\frac{1}{2}T_o$, later at t_1, because the blocking diode D4b prevents the inductor current i_L from going positive.

t_{S4off}: Controlled zero-current turn off of S4

Switch S4 can be turned off after D4b begins blocking at t_1 and at least t_q before the D2 $\rightarrow$S1 commutation is initiated at $t_{S1on} = t_2$.

t_2: Initiation of D2$\rightarrow$S1 commutation

A hard-switched commutation of I_s from D2 to S1 occurs at $t_{S1on} = t_2$ as S1 is gated on and D2 reverse biases. It should be noted that this impresses an extremely high *di/dt* stress on the off-going D2.

t_3: Initiation of S1$\rightarrow$D2 commutation

The process of commutating I_s from S1 to D2 is initiated at t_3 by gating on S3 to form a loop comprised of the capacitor, S1, S3, S3b, and the inductor. It should be noted that the subsequent pole voltage transition actually occurs more than one quarter of a resonant cycle later at t_5.

t_4: Natural S1$\rightarrow$D1 commutation

A natural commutation from S1 to D1 occurs at t_4 as i_L exceeds I_s. By Kirchoff's current law, i_{S1} would otherwise be forced negative. This is the initial boundary of a window during which S1 can be turned off with minimal stress.

t_{S1off}: Controlled zero-current turn off of S1

Once i_{S1} is zero, S1 can be turned off with minimal stress. The turn off process should be completed prior to t_5, thus t_{S1off} should precede t_5 by at least t_q.

t_5: Natural D1$\rightarrow$D2 commutation

A natural commutation of $i_L - I_s$ from D1 to D2 occurs at t_5 as i_L falls below I_s. It is assumed that t_5 is the final boundary of a window during which S1 can be turned off under zero current. Between t_5 and t_6, the resonant tank is part of a loop that also includes D2, the dc voltage source V_s, S3 and D3b. The product $i_L V_s$ during this interval represents a net power flow into the resonant tank. This power flow, which cannot be offset by an opposite flow, leads to an incremental increase in stored energy.

t_6: Natural extinguishing of S3 current

Because both S3 and D3b carry i_L, which is blocked from going negative by D3b, the S3 current i_{S3} extinguishes naturally at t_6.

t_{S3off}: Controlled turn off of S3

Once i_{S3} has reached zero, S3 can be turned off with minimal stress.

The next PWM cycle can be initiated once the physical turn-off process for S3 is completed at t_6 and t_q.

A special start-up sequence is required for the BRDCY, because the state-plane trajectory does not approach the origin. Fortunately, a relatively simple sequence is possible. Starting from the origin of the state plane, the dashed trajectory in Fig. 3.2 is followed by gating on S1 and S4. This trajectory terminates naturally at the point labeled t_1&t_2, as the blocking diode D4b prevents the second half of a resonant cycle. Once at this point, the sequence described above can be followed readily starting at t_2.

3.3 Concept Simulation

Concept simulations of this topology and strategy have been performed to validate the previous analysis and to provide a basis for more detailed simulations to be used in design. A schematic of the circuit entered in Saber is shown in Fig. 3.4. Each switch in this simulation is modeled as an IRGPC50F IGBT, which has voltage and current ratings of 600 V and 280 A, respectively. The tail interval is programmed to be approximately 270 ns, which is similar to the tail interval observed in the MCT models provided by Harris. The diode is modeled as an ESM 244_600, which has voltage and current ratings of 600V and 800A, respectively. This diode is particularly useful due to its relatively rapid reverse recovery characteristics and reverse recovery current limit of 6 A, which are representative of diodes that are likely to be used in an implementation. The voltage source and current source are simple dc sources without ac noise. The capacitors and inductors are also basic devices with initial conditions set to zero. All resistor components are set to the indicated values without thermal effects being simulated.

The converter was simulated under a variety of load conditions ranging from I_s = 20 A to I_s = 150 A. Operation at I_s = 50 is depicted in Fig. 3.5, which shows the auxiliary voltage v_{aux}, the pole voltage v_{pole}, the resonant inductor current i_L, the resonant capacitor

voltage v_C, the upper main switch current i_{S1}, the lower auxiliary switch current i_{S2}, and the corresponding switch gating signals. To facilitate comparison between these simulation waveforms and the previous analysis, the simulation time of several of the key instants are listed in Table 3.1. The overall similarity between these waveforms and those in Figs. 3.2 and 3.3 indicates that the analysis is correct. Although these simulation results are for the second PWM cycle (simulation starts at $t = 0$), they are representative of cycles at and beyond the 100th. This is of note, as these results do not show the trapped energy problem to be as significant as the earlier analysis had indicated. The discrepancy is likely due to the presence of substantial energy dissipation in the modeled diodes and to a lesser extent the switches. This dissipation is apparent in Fig. 3.8, which indicates that there is nearly 1 mJ (=½(10 μs)(200 W)). Due to the relatively low dc input voltage and ac output current this represents a fairly significant energy loss.

A practical problem that is apparent in the simulation occurs at turn on of the main switch S1 at time t_2. A peak switch current of approximately 1.5 times the load current is reached in a very short time. The additional current component is due to reverse recovery of the opposite main diode D2. While simulation using models of commercial IGBTs and diodes indicates an undesirable but survivable condition, use of MCTs is likely to result in a *di/dt* that is great enough to cause catastrophic failure of the diode.

Table 3.1 Comparison of Analysis and Simulation Times

Analysis Instant	t_0	t_1	t_2	t_3	t_4	t_5	t_6
Simulation Time (μs)	180	188	220	270	272	275	280

3.4 CONTROL SYNTHESIS

Although continued uncertainty about the trapped energy problem may make control synthesis premature, the simplicity of the control makes any investment in time relatively small. In fact, the primary advantage of this topology/strategy is the incredible simplicity of its control. Initiation of the voltage reversal prior to the hard-switched D2→S1 commutation should occur at least one-half resonant period plus an allowance for one circuit-commutated turn-off time t_q and signal propagation delays. Turn off of S1 between t_4 and t_5 can be timed relative to t_3 (t_{S3on}) using either a feedback/feedforward

control or a quarter-resonant period delay. For feedback/feedforward control, t_4 would be calculated as

$$t_4 = t_3 + \left[\frac{T_0}{2\pi}\sin^{-1}\left(\frac{I_s}{I_{L,peak}}\right)\right] \qquad 3.4\text{-}1$$

where the resonant period T_0 could be established via feedback or from design/tested parameters, I_s would be fed forward from an expected load current sensor, and $I_{L,peak}$ would be fedback as a measured value. Such feedback appears to be necessary, as the steady-state value of this variable depends upon the degree of the trapped energy. The simpler approach of quarter-resonant period delay carries the usual caution that it provides the least margin on t_q. With either approach, appropriate signal propagation delays should be taken into account.

3.5 Design Optimization and Trade-offs

Due to the trapped energy issue, closed-form design optimization does not appear to be possible for this topology. Instead, it is recommended that a new strategy be developed or detailed computer simulation using Saber be performed.

3.6 Conclusions

This design requires more detailed analysis and simulation than any of the other converters, due to the uncertainties surrounding the trapped energy problem. Basic analysis suggests that excessive component stresses are likely. Simulations at relatively low power, however, indicate that typical resonant circuit parasitics are sufficient to limit the voltage and current extremes to manageable levels.

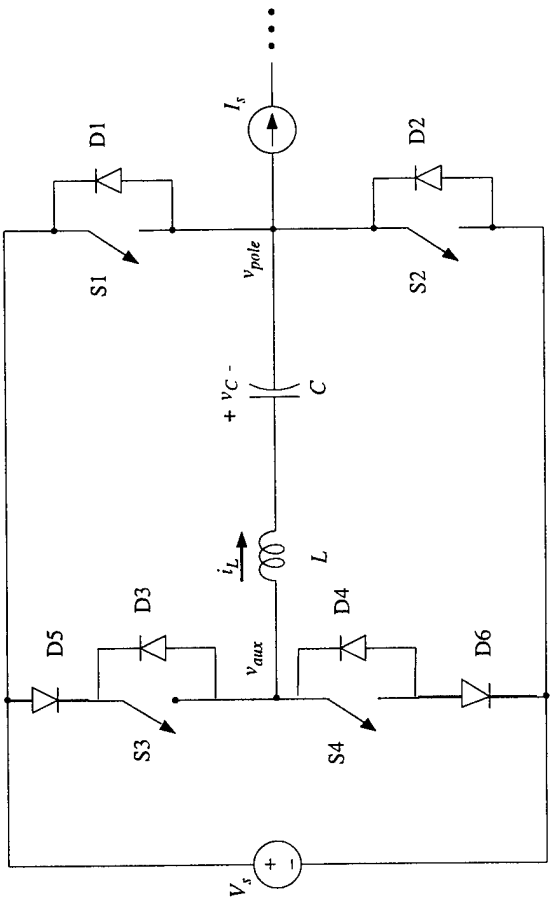

Figure 3.1 BRDCY Basic Circuit

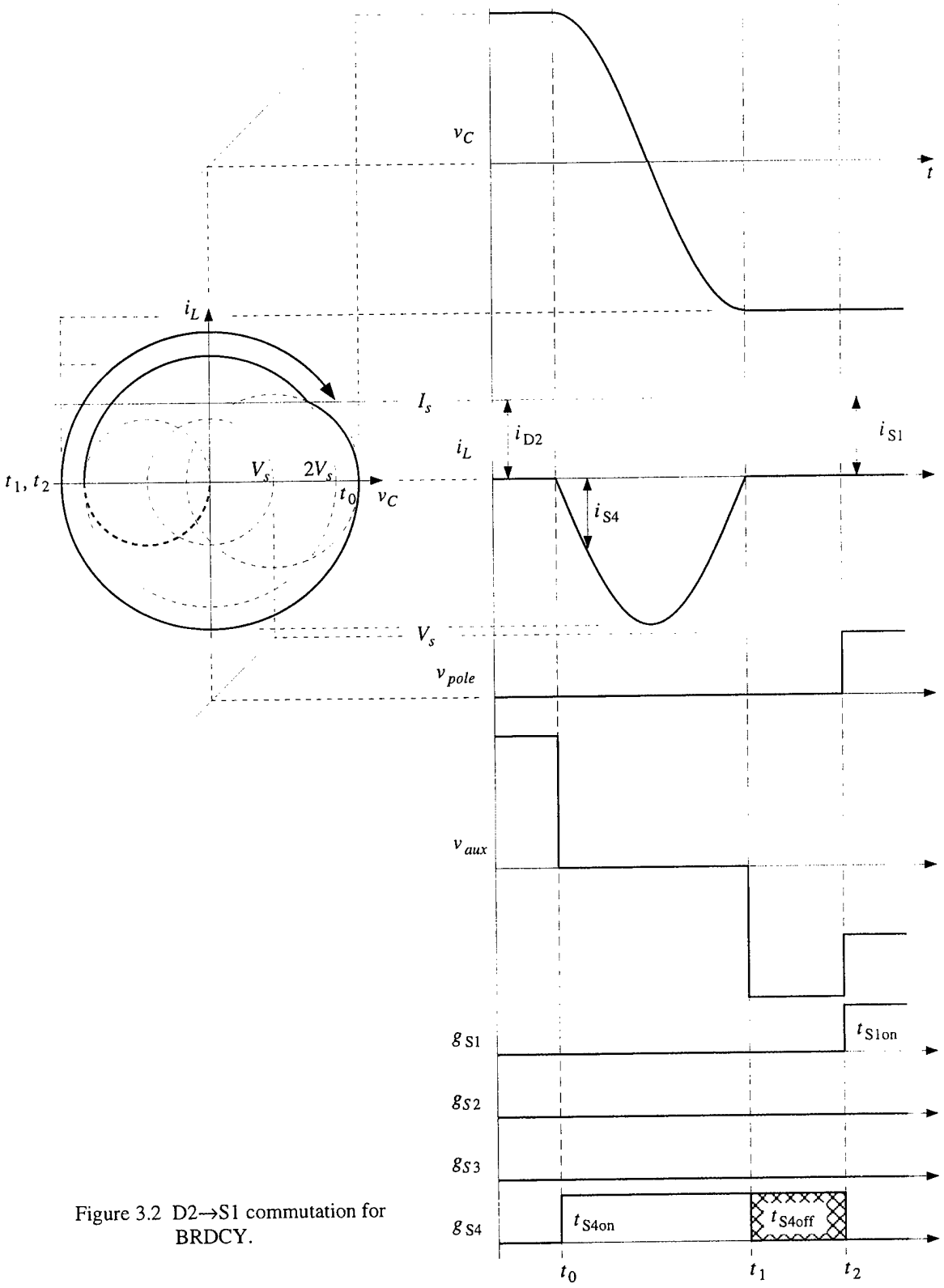

Figure 3.2 D2→S1 commutation for BRDCY.

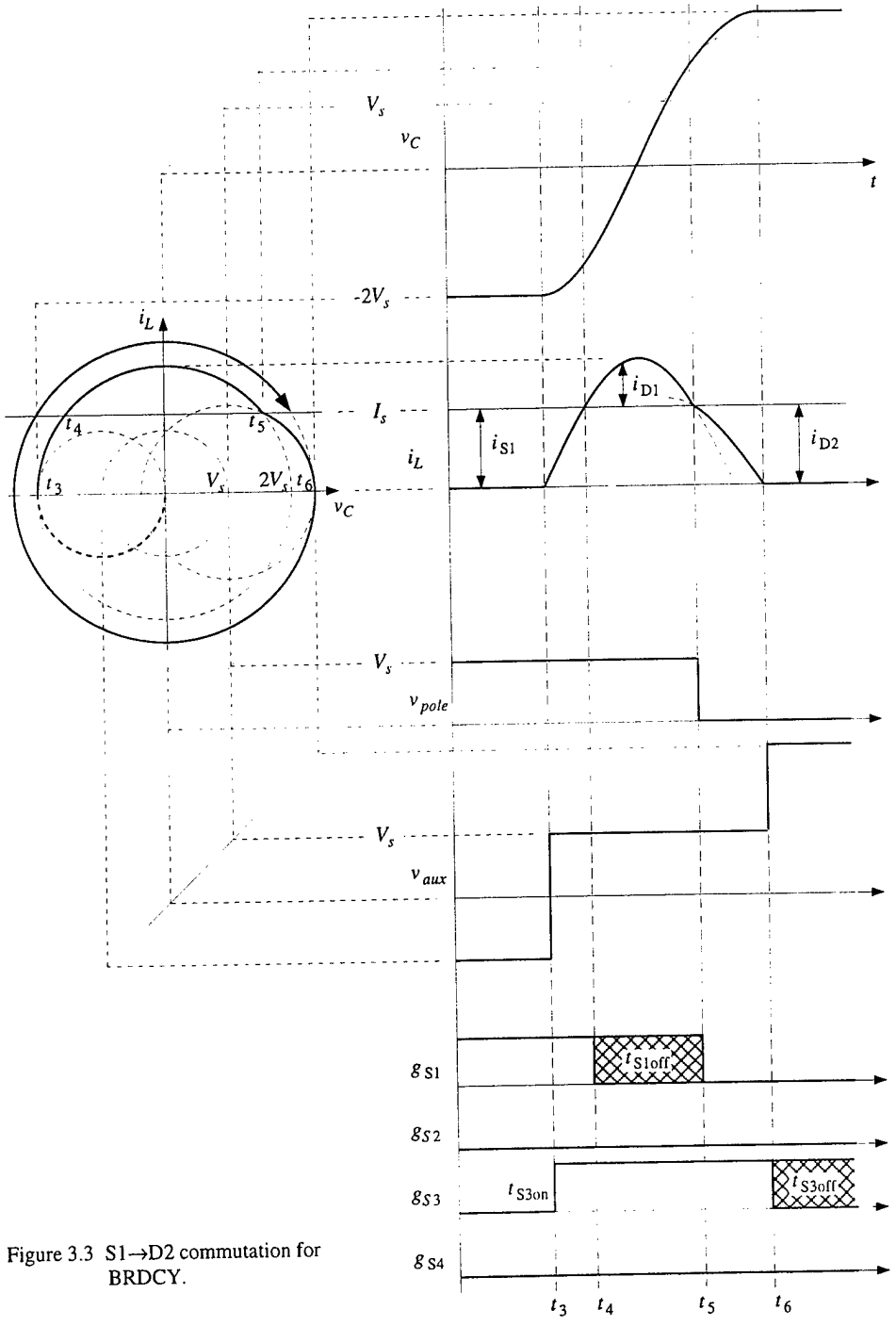

Figure 3.3 S1→D2 commutation for BRDCY.

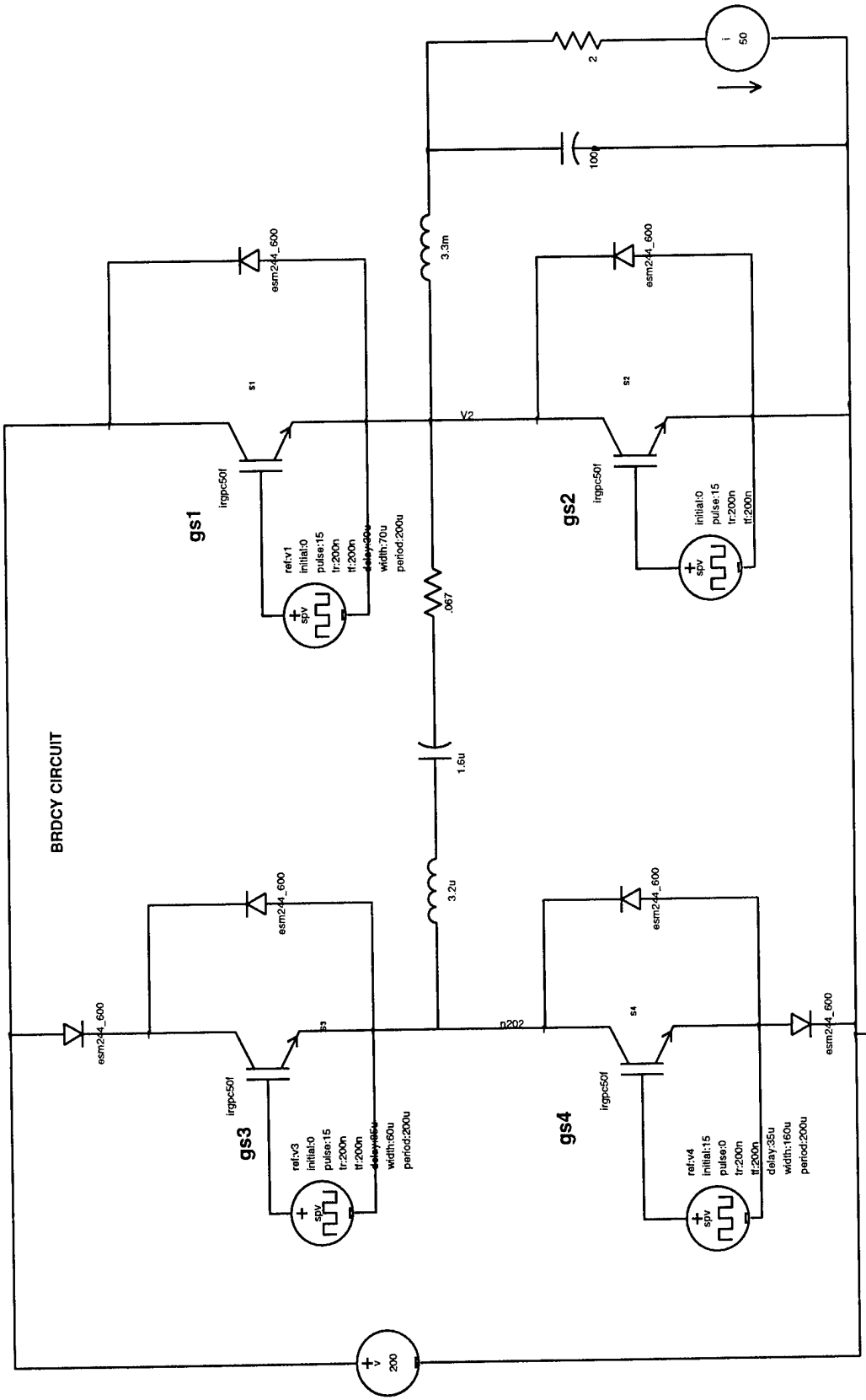

Figure 3.4 BRDCY Circuit

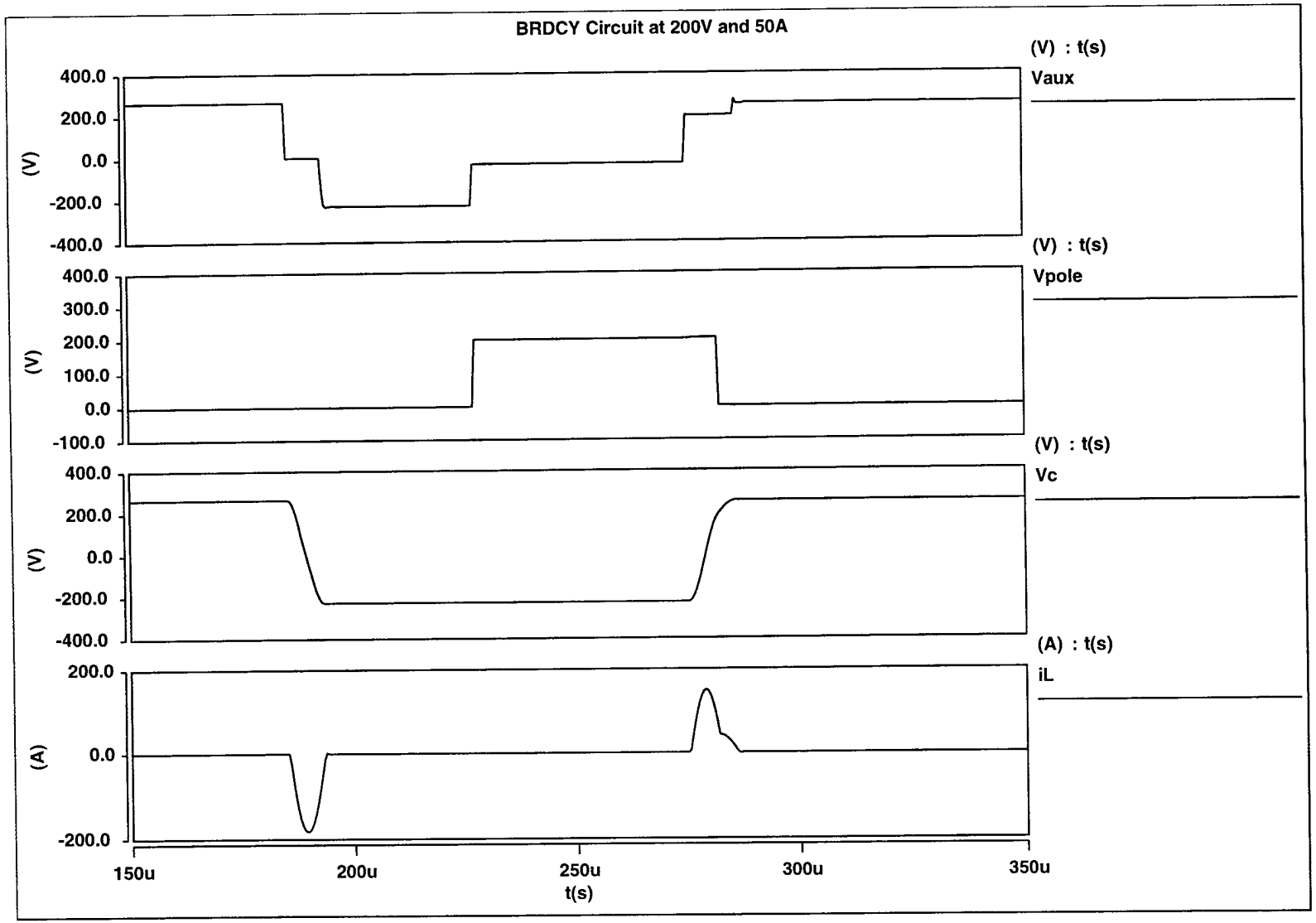

Figure 3.5 BRDCY Circuit Resonant Waveforms

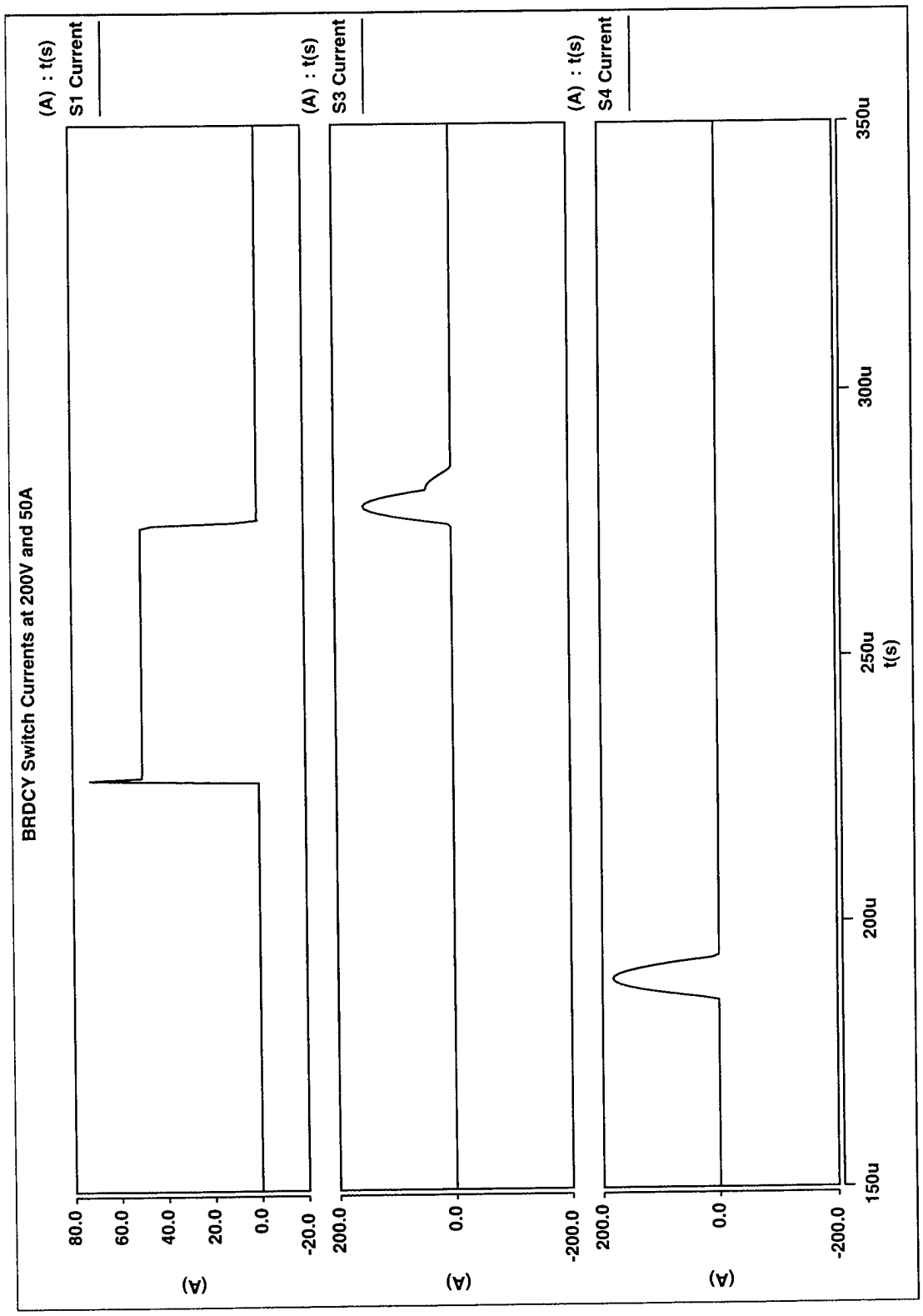

Figure 3.6 BRDCY Switch Currents

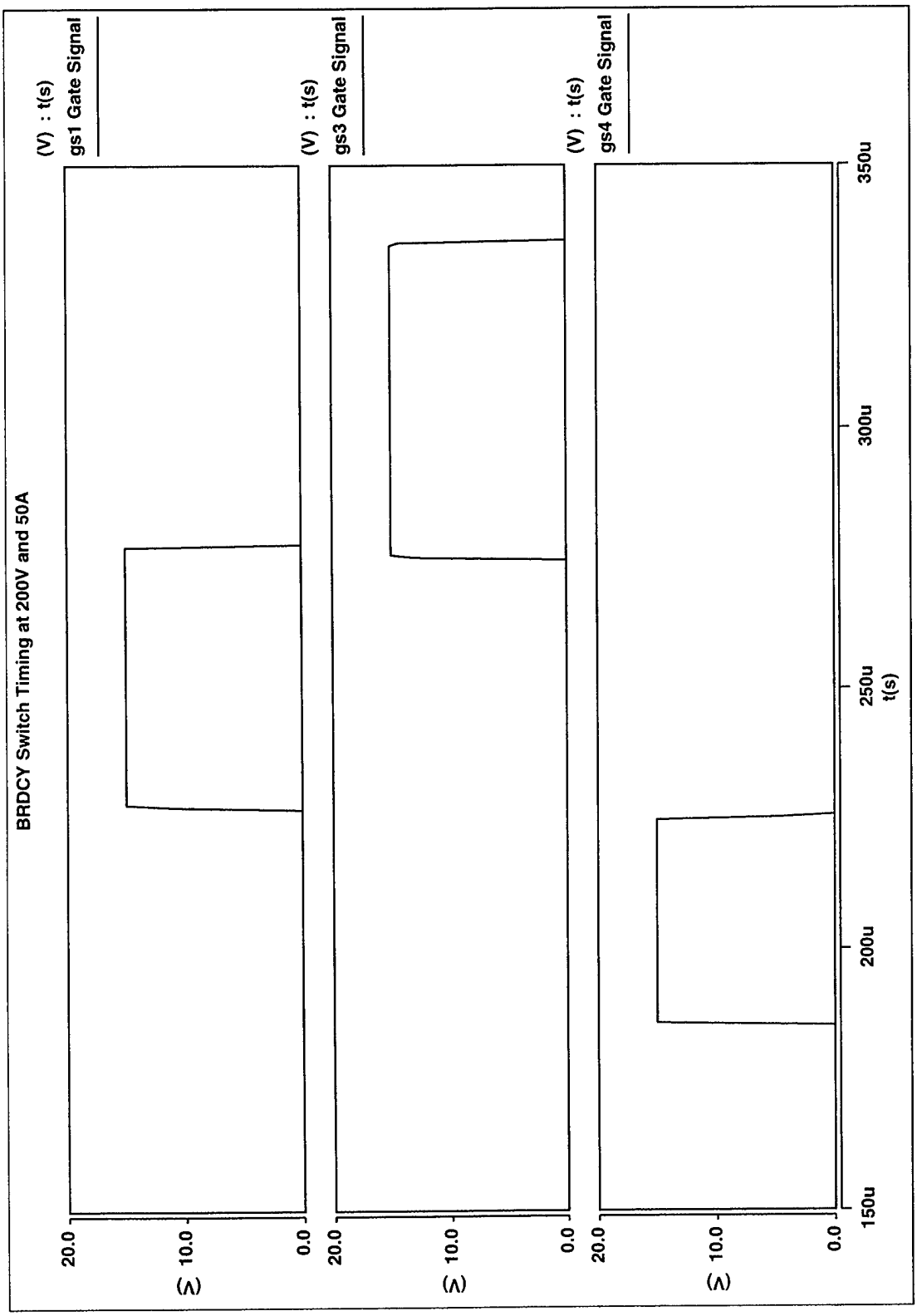

Figure 3.7 BRDCY Switch Timing

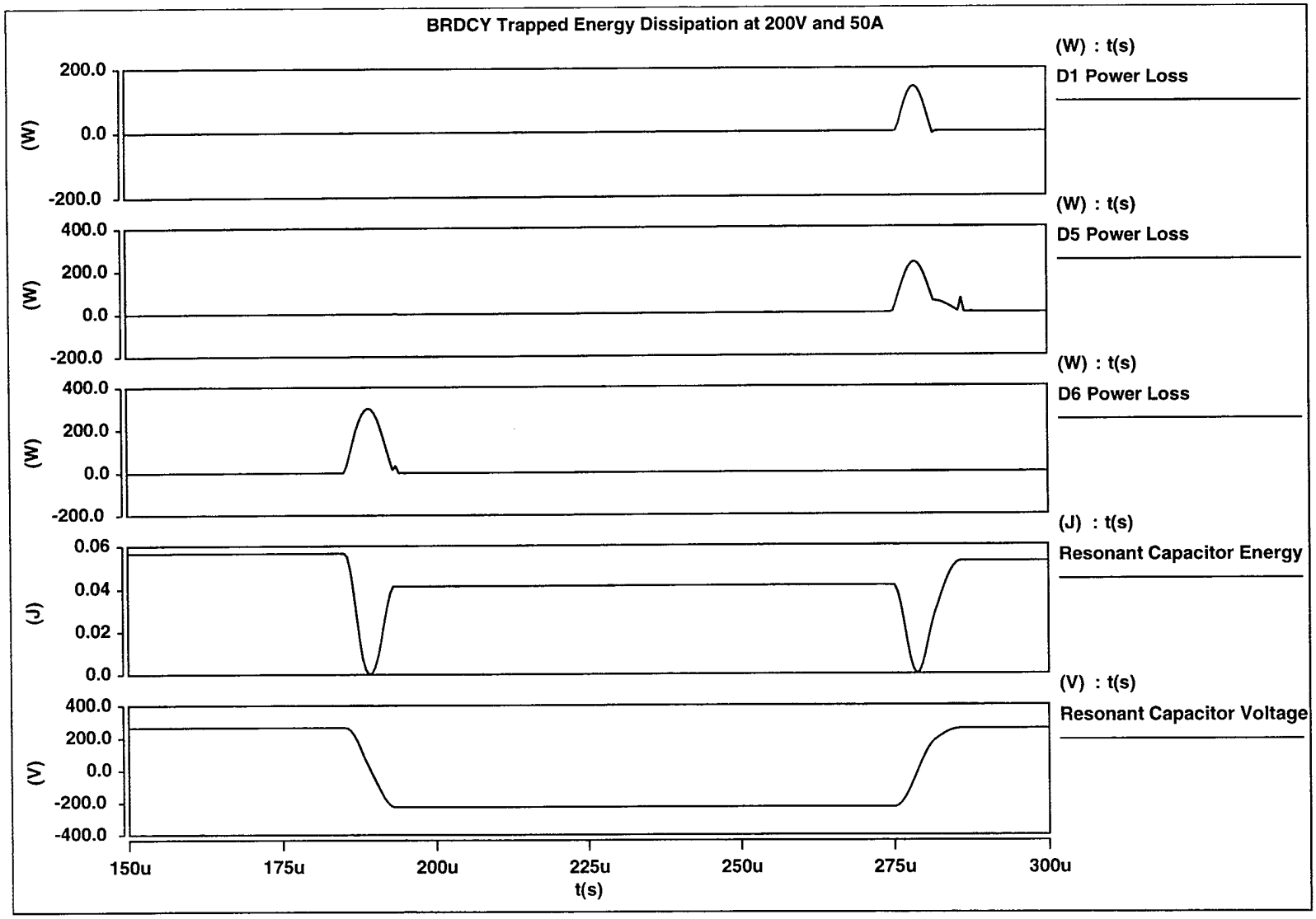

Figure 3.8 BRDCY Trapped Energy Dissipation

CHAPTER 4
RESONANT BRIDGE WITH ZERO-CURRENT TURN-OFF

4.1 INTRODUCTION

In this chapter, a new switching control strategy is described for the resonant bridge topology introduced in Chapter 2 and shown again in Figure 4.1. The turn-around time of the new strategy is shorter than that of the MLZDCB strategy described in Chapter 2, because zero-current turn on is sacrificed to eliminate approximately half of a resonant cycle. Moreover, this strategy allows a completely relative-time control, which is simpler than that described previously. The principal drawback of this strategy is the rapid turn-on of the main MCTs and the accompanying stress on the opposite off-going diode. Specific characteristics of the diodes necessary to handle these large stresses are discussed.

4.2 WAVEFORM ANALYSIS

The capacitor voltage v_C, inductor current i_L, pole voltage v_{pole}, and auxiliary voltage v_{aux}, waveforms along with the switch gating signals are shown in Figs. 4.2 and 4.3. As indicated in these figures, which represent the D2→S1 and S1→D2 commutations, there are ten instances of interest during each PWM cycle: t_0 through t_7, t_{S1off}, and t_{S3off}. In addition, this converter requires a special start-up sequence, as the state-plane trajectory never approaches the origin (i.e., a de-energized state). The additional startup sequence utilizes switch S4 and S1 to establish the initial v_C of Fig. 4.2.

t_0: Controlled turn on of S1 (nearly instant D2→S1 commutation)

Commutation of the load current I_s from D2 to S1 is accomplished by a hard-switched turn on of S1; this would put considerable *di/dt* stress on D2. Because v_C is initially charged to a positive value midway between 0 and the dc input voltage V_s and the resonant components are in loop with S1 and D3, there is negative resonant inductor current pulse i_L.

t_1: Natural turn off of D3

The resonant current is blocked from going positive by D3. At this point the initially positive value of v_C has been reversed to a negative value.

t_2: Initiation of S1→D2 commutation

Commutation of I_s from S1 to D2 commences at t_2 by gating on S3. This results in a positive resonant inductor current pulse i_L, as the resonant components are in a loop with S1 and S3 and v_C is initially negative.

t_3: Natural S1→D1 commutation

Once i_L reaches the level of I_s, the difference of these currents commutates from S1 to D1, setting the stage for zero-current turn-off of S1.

t_{S1off}: Controlled zero-current turn off of S1

Switch S1 is turned-off at a convenient time after $i_L - I_s$ has commutated to D1. The turn-off process should be completed before t_4, or else S1 might be latched on again by a forward current. To ensure that this condition is avoided, S1 should be turned off no later than t_q before t_4.

t_4: Start of constant i_L (linear v_C) interval

Once the resonant inductor current has fallen to the level of the load current I_s and S1 is off, diode D1 turns off naturally. The load current does not begin to commutate to D2, however, because v_C being less than V_s would cause i_L to increase, thereby requiring i_{D2} to become negative. Instead D2 remains off, and i_L is fixed at I_s. This positive current charges the capacitor linearly until v_C reaches a value of V_s and v_{pole} reaches zero.

t_5: Natural L→D2 commutation

Once v_{pole} reaches zero, D2 becomes forward biased and begins to pick up the output current I_s as i_L decreases. Note v_C continues to increase toward its peak value.

t_6: Natural S3→D3 commutation

Once i_L has reached zero and begins to go negative, it commutates from S3 to D3.

t_{S3off} : Controlled zero-current turn off of S3

With zero current through S3, this device can be turned off with minimal stress.

t_7: Completion of S1→D2 commutation

Once ½ of a resonant cycle is completed, the resonant inductor current returns to

zero and D3 turns off naturally.

The next PWM cycle can be initiated once the physical turn-off process for S3 is completed.

In order to establish the appropriate initial conditions for the first commutation cycle of this strategy, a startup sequence is required. Starting from the origin of the state plane, S4 and S1 are gated on simultaneously, so that the resonant circuit follows the dashed trajectory in Fig. 4.2. To terminate this trajectory on the solid trajectory, which subsequently terminates at t_1, S4 is turned off after approximately $T_o/12$, while S1 remains on. The one-time hard turn off of S4 should not be deleterious.

4.3 Concept Simulation

Concept simulations of this topology and strategy have been performed to validate the previous analysis and to provide a basis for more detailed simulations to be used in design. A schematic of the circuit entered in Saber is shown in Fig. 2.4. Each switch in this simulation is modeled as an IRGPC50F IGBT, which has voltage and current ratings of 600 V and 280 A, respectively. The tail interval is programmed to be approximately 270 ns, which is similar to the tail interval observed in the MCT models provided by Harris. The diode is modeled as an ESM 244_600, which has voltage and current ratings of 600 V and 800 A, respectively. This diode is particularly useful due to its relatively rapid reverse recovery characteristics and reverse recovery current limit of 6 A, which are representative of diodes that are likely to be used in an implementation. The voltage source and current source are simple dc sources without ac noise. The capacitors and inductors are also basic devices with initial conditions set to zero. All resistor components are set to the indicated values without thermal effects being simulated. The output inductor is set to an initial value of steady-state load current and the resonant capacitor is set to an initial value of voltage as discussed in Section 4.2.

The converter was simulated under a variety of load conditions ranging from I_s = 20 A to I_s = 150 A. Operation at I_s = 50 is depicted in Figs. 4.5-4.7, which show the auxiliary voltage v_{aux}, the pole voltage v_{pole}, the resonant inductor current i_L, the resonant capacitor voltage v_C, the upper main switch current i_{S1}, the upper auxiliary switch current i_{S3}, and the corresponding switch gating signals. To facilitate comparison between these simulation waveforms and the previous analysis, the simulation time of several of the key

instants are listed in Table 4.1. The overall similarity between these waveforms and those in Figs. 4.2 and 4.3 indicates that the analysis is correct. The currents through S1 and S3 attain peak values of approximately 1.5 times the load current. The reverse recovery of diode D2 at the hard turn-on of S1 is apparent in the simulation results and raises concerns. Device characteristics required to account for a hard turn-off of D2 are discussed in Section 4.5.

The reverse recovery of diode D3 is readily apparent at time t_7 in the simulation results. This recovery occurs when i_L returns to zero. The effect of this recovery is seen as a variation on v_{aux}. This does not appear to have a negative effect on the circuit operation. Depending on the current sensing method chosen, as discussed in Appendix B, this variation could impact circuit operation.

Table 4.1 Comparison of Analysis and Simulation Times

Analysis Instant	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7
Simulation Time (μs)	408	413	430	431	435	437	439	445

4.4 CONTROL SYNTHESIS

A relative time-control method can be implemented readily for this strategy. The key points of concern within this strategy are the turn off of S1 and S3 at t_{S1off} and t_{S3off}, respectively. Both of these times can be determined using a relative-time control method: one relative to a controlled switching instant and the other relative to the zero-crossing point of resonant inductor current i_L. The second case requires that i_L be sensed; various methods for doing this are discussed in Appendix B.

The turn off of S1 must occur while i_L exceeded I_s and D1 rather than S1 is carrying their difference. This constrains t_{S1on} to the interval (t_3, t_4) An additional constraint is imposed by the circuit-commutated turn off time t_q of the MCT. In particular, the MCT should be gated-off at least t_q seconds before t_4, to ensure that the device is not latched on inadvertently by a re-impressed forward voltage. These are the same conditions described in Chapter 2 for the MLZDCB, and as with that topology/strategy, there are several design choices that require a trade-off between simplicity of implementation and conservatism in accommodating large values of t_q. The least simple but most accommodating design requires sensing the peak amplitude of the

resonant inductor current $I_{L,peak}$ during the half-resonant cycle associated with the preceding D2→S1 commutation. In addition, I_s would have to be sensed, but this is expected, as current measurements are required for most advanced application controllers and/or short-circuit protection. Given these two values and the resonant period,[3] the value of t_3 can be calculated relative to t_2 using an analytical expression for the intersection of the i_L sine wave with the I_s constant

$$t_3 = t_2 + \left[\left(T_0/2\pi\right)\sin^{-1}\left(\frac{I_s}{I_{L,peak}}\right)\right] \qquad 4.4\text{-}1$$

The result of this calculation would be used as the controlled turn-off instant t_{S1off} after increasing or decreasing it slightly to accommodate signal propagation delays. In particular, an intrinsic software/hardware delay, which makes the actual t_2 slightly later than t_{S3on}, would have to be added to the calculated t_3, while a similar delay which makes t_{S1off} slightly later than t_3, would have to be subtracted.

A controller at the opposite extreme in terms of simplicity and conservatism would require only an estimate of T_o. In this case, the instant at which i_L peaks would be calculated as $t_2 + \frac{1}{4}T_o$. From this calculated instant, t_{S1off} would again be selected based on expected propagation delays.

The controlled zero-current turn off of S3 is relatively easy compared to the turn off of S1 just described. In particular, there is significantly more time available to complete the turn off ($\frac{1}{2}T_o$) and this instant can be relative to t_6, which is zero crossing of i_L and therefore determined readily.

4.5 Design Optimization and Trade-Offs

Design optimization for the SSM parallels that for the MLZDCB described in Chapter 2. In fact, it is shown that exactly the same values of L and C are optimal for both converters. The hard turn-on of the SSM, however, may lead to additional switching losses and requires more careful selection of the main diodes, as discussed subsequently.

In the analysis described in Section 4.2, specific values for the resonant inductor L and capacitor C were not necessary, as a normalized state-plane was employed. In the

[3] The resonant period T_o can be calculated approximately using the design or as-tested values of the

design of a practical converter, however, the selection of L and C is critically important to obtain "optimal" converter performance and avoid excessive component stress. The selection of L and C is done best by a process in which "optimal" converter performance is defined explicitly (mathematically). Such a process is described here and is very similar to that described for the MLZDCB in Chapter 2.

Ultimately, the process of selecting L and C will require identifying the maximum dc input voltage V_s and the maximum (instantaneous) ac output current I_s specifications for the converter as well as the circuit-commutated turn-off time t_q of the main and auxiliary switches. These values then represent design parameters. Within the process, it is assumed there are two primary criteria for optimal performance of the converter. The first is related to t_q of the main switches. In particular, the window in which to turn off S1 under zero current must be greater than t_q by up to a factor of two, depending upon the gating control method (see previous section). This criterion is necessary to avoid inadvertent turn on of a main switch and will lead to a mathematical relationship between the resonant period T_o, which is related to L and C ($T_o=(LC)^{1/2}/2\pi$) and the ratio of the output current I_s to the peak resonant inductor current $I_{L,peak}$; this ratio is a key design variable and will be referred to as m. The second criterion is that the additional conduction losses in the auxiliary and main switches due to the resonant current pulses should be minimal. This criterion will be met explicitly by minimizing a mathematical expression for the additional losses with respect to the design variable $m = I_s/I_{L,peak}$. The design process will now be described.

The starting point is determining the relationship between T_o and $m = I_s/I_{L,peak}$, given the constraint $T_{S1off} = t_4 - t_3 \geq t_q$. The boundaries of the T_{S1off} window are the intersections of the constant output current with the resonant inductor current pulse. These intersections can be expressed

$$I_s = I_{L,peak} \cos\left(\frac{2\pi t}{T_0}\right) \qquad 4.5\text{-}1$$

where it is assumed that the time reference is midway between t_3 and t_4. Solving for t

$$t = \frac{T_0}{2\pi} \cos^{-1}\left(\frac{I_s}{I_{L,peak}}\right) \qquad 4.5\text{-}2$$

resonant components or it could be measured during one of the half resonant period pulses.

This implies that

$$T_{off} = t_4 - t_3 = \frac{T_0}{\pi}\cos^{-1}\left(\frac{I_s}{I_{L,peak}}\right) \qquad 4.5\text{-}3$$

Denoting the ratio of I_s to $I_{L,peak}$ as m

$$T_{off} = \frac{T_0}{\pi}\cos^{-1} m \qquad 4.5\text{-}4$$

Ultimately, T_{off} will be set based on the design parameter t_q, and m will be selected through an optimization (minimization) process, so this equation will provide the desired resonant frequency that, in turn, will provide L and C.

Although the resonant circuit is used to reduce switching losses of the pole switches, its resonant current pulses will result in new losses in the auxiliary circuit and greater conduction losses in the main switches. Intuitively, the magnitude of the additional losses will be related to the magnitude of the resonant current pulses, which can be expressed in terms of the design parameter I_s and design variable m (i.e., I_s/m). The exact expression for the additional losses can be derived in two parts. First the new losses will be expressed for the auxiliary circuit, which includes an auxiliary switch (corresponding to either the controlled device or the diode), the resonant inductor, and resonant capacitor. Second, the conduction losses in excess of the hard-switched conduction losses of the main switches will be expressed. In both cases, it assumed that the conduction losses can be expressed as the product of a constant voltage drop times an appropriate current. This constant-voltage model is much simpler to work with than a more realistic one that includes a constant on-state voltage for the switch plus an ohmic term Ri_L for the passive components. More accurate modeling is probably done better using a circuit simulation program. In any event, the auxiliary circuit voltage drop will be denoted V_c. The drop for the main switches will be denoted as V_c/k, where k typically lies between 2 and 4, as the "equivalent power" loss in the auxiliary circuit passive components corresponds to between ½ and ¾ of the auxiliary circuit losses.

The auxiliary circuit losses can now be expressed

$$E_{aux} = \int_{t_0}^{t_1} V_c|i_L|dt + \int_{t_2}^{t_7} V_c|i_L|dt \qquad 4.5\text{-}5$$

$$= V_c\left[\int_{t_0}^{t_1} -i_L dt + \int_{t_2}^{t_6} i_L dt + \int_{t_6}^{t_7} -i_L dt\right] \qquad 4.5\text{-}6$$

Because i_L flows through the resonant capacitor, the various integrals of i_L in this expression can be related to the capacitor voltages at the bounds of integration

$$E_{aux} = V_c[-v_C(t_1) + v_C(t_0) + v_C(t_6) - v_C(t_2) - v_C(t_7) + v_C(t_6)] \qquad 4.5\text{-}7$$

This expression can be simplified by noting that $v_C(t_0) = -v_C(t_7)$ and $v_C(t_1) = v_C(t_2)$

$$E_{aux} = V_c C[2v_C(t_6) - 2v_C(t_1)] \qquad 4.5\text{-}8$$

To get back to an expression in terms of design parameters, note that $v_C(t_6)$ corresponds to V_s plus the increase in capacitor voltage due to the transfer of energy from the inductor to the capacitor between t_5 and t_6 (i.e., $(L/C)^{1/2} I_s$). Continuation of the resonant cycle between t_6 and t_7 leads to the following relationship,

$$v_C(t_7) = V_s - \sqrt{\frac{L}{C}} I_s \qquad 4.5\text{-}9$$

This is the voltage at the beginning of the next PWM cycle. The voltage reversal process at the start of that cycle leads to $v_C(t_1) = -V_s + (L/C)^{1/2} I_s$. Substituting these expressions for $v_C(t_6)$ and $v_C(t_2)$ yields

$$E_{aux} = 4V_c C V_s \qquad 4.5\text{-}10$$

Interestingly, the losses in the auxiliary circuit appear to be independent of the output current.

While the last expression is in terms of design parameters V_c and V_s and a design objective C, it can be written in terms of the design variable m by using the following relationship obtained by equating energy in the inductor midway between t_0 and t_1 to the energy in the capacitor at t_1

$$\sqrt{L} I_{L,peak} = \sqrt{C}\left(V_s - \sqrt{\frac{L}{C}} I_s\right) \qquad 4.5\text{-}11$$

$$V_s = \sqrt{\frac{L}{C}} I_{L,peak} + \sqrt{\frac{L}{C}} I_s \qquad 4.5\text{-}12$$

$$= \sqrt{L/C}(1+m)I_{L,peak} \qquad 4.5\text{-}13$$

Substituting the last expression for V_s yields

$$E_{aux} = 4V_c C\sqrt{L/C}(1+m)I_{L,peak} \qquad 4.5\text{-}14$$

$$= 4V_C\sqrt{LC}(1+m)I_{L,peak} \qquad 4.5\text{-}15$$

$$= \frac{4V_c T_0}{2\pi}(1+m)I_{L,peak} \qquad 4.5\text{-}16$$

4.5-17

This is exactly the same expression that was obtained for the MLZDCB.

The additional main switch losses occur when these devices carry resonant current with magnitude exceeding the magnitude of the output current. This occurs between t_3 and t_4 as well as in an interval lying within t_6 and t_7. For every other time during a resonant cycle, an increase (decrease) in main switch current is countered by a decrease (increase) at another time. The additional conduction losses in the main switches can be expressed

$$E_{main} = 2\int_{t_3}^{t_4}\frac{V_c}{k}\left[I_{L,peak}\cos\omega t - I_s\right]dt \qquad 4.5\text{-}18$$

$$= \frac{2V_c}{k}\left[\frac{1}{\omega}I_{L,peak}\sin\omega t\Big|_{t_3}^{t_4} - I_s t\Big|_{t_3}^{t_4}\right] \qquad 4.5\text{-}19$$

$$= 2\frac{V_c}{k}\left[\frac{T_0}{2\pi}I_{L,peak}(\sin\omega t_4 - \sin\omega t_3) - I_s(T_{off})\right] \qquad 4.5\text{-}20$$

$$= \frac{2V_c}{k}\left[\frac{T_0}{2\pi}I_{L,peak}2\sqrt{1-m^2} - I_{L,peak}m\frac{T_0}{\pi}\cos^{-1}m\right] \qquad 4.5\text{-}21$$

$$= \frac{2V_c}{k}\left[\sqrt{1-m^2} - m\cos^{-1}m\right]\frac{T_0 I_{L,peak}}{\pi} \qquad 4.5\text{-}22$$

$$= \frac{2}{\pi}\left(\sqrt{1-m^2} - m\cos^{-1} m\right)\frac{V_c}{k} I_{L,peak} T_0 \qquad 4.5\text{-}23$$

Once again, this expression is identical to that for the MLZDCB.

The total additional losses due to the use of auxiliary resonant circuit can be expressed as the sum of the two separate components and is the same as that for the MLZDCB

$$E_{loss} = \frac{2}{\pi}\left[1 + m + \frac{\sqrt{1-m^2} - m\cos^{-1} m}{k}\right] T_0 V_c I_{L,peak} \qquad 4.5\text{-}24$$

Given I_s, T_{off}, and now V_c as design parameters, this expression can be normalized as

$$E_{normalized} = \frac{E_{loss}}{2V_c I_s T_{off}} \qquad 4.5\text{-}25$$

$$= \frac{1 + m + \left(\dfrac{\sqrt{1-m^2} - m\cos^{-1} m}{k}\right)}{m\cos^{-1} m} \qquad 4.5\text{-}26$$

This expression relates the additional losses due to the auxiliary circuit to the design variable m (and the design parameter k). A family of plots of $E_{normalized}$ vs. m is shown in Fig. 4.8 for k ranging from 1 to 5. From these plots, it can be deduced that the optimal value of M is in the interval [0.5,0.7]. The specific design value for m is denoted as M. Once m has been selected, the resonant period can be calculated after manipulating (4.5-4).

$$T_0 = \frac{\pi T_{off}}{\cos^{-1} M} \qquad 4.5\text{-}27$$

Because $T_o = 2\pi(LC)^{1/2}$, there is now one equation relating the desired parameter values, L and C. A second equation comes from the relationship between $I_{L,peak}$ and V_s discussed previously; $I_{L,peak}$ in this equation can now be replaced by MI_s. The simultaneous solution of these two equations yields the following expressions for L and C

$$L = \frac{V_s T_{off}}{2MI_s \cos^{-1} M} \qquad 4.5\text{-}28$$

$$C = \frac{MT_{off} I_s}{2V_s \cos^{-1} M} \qquad 4.5\text{-}29$$

These formulas can be used to determine values for the resonant inductor and capacitor that can then be refined through simulation and/or experimentation.

The design optimization just described does not address the impact of turn-around time on converter performance, as the resonant period was determined based on minimizing auxiliary circuit losses. To avoid the deleterious effects of turn-around time on bus utilization and THD it may be necessary to accept additional losses. The actual losses will also be higher due to turn-on losses that have not been modeled.

The SSM offers a reduced turn-around time when compared to the MLZDCB (Chapters 2) and the ACSMM (Chapter 5), because zero-current turn-on of the main switches is sacrificed. It is anticipated that MCTs can accommodate full-load turn on readily, as it has been stated that these devices can support "infinite" *di/dt*. There is, however, a concern that the corresponding turn off of the opposite diodes will be too abrupt for existing devices. More specifically, presently available diodes have not been designed to accommodate a severe reverse-recovery transient. This recovery could result in a significant reduction in the switch utilization of this strategy due to the large recovery currents that could result. Additionally, failure of the diode could result from the abrupt recovery.

4.6 Conclusion

This strategy resolves some of the issues associated with bus utilization and THD that resulted from the resonant bridge of Chapter 2 by reducing the turn-around time by ½ of the resonant period. The loss of zero-current turn-on is not expected to be a significant contributor to power loss within this strategy as long as diodes with a good compromise of rapid recovery and minimal on-state voltage drop are utilized. This strategy appears to be a viable option for implementation within a zero-current PWM strategy.

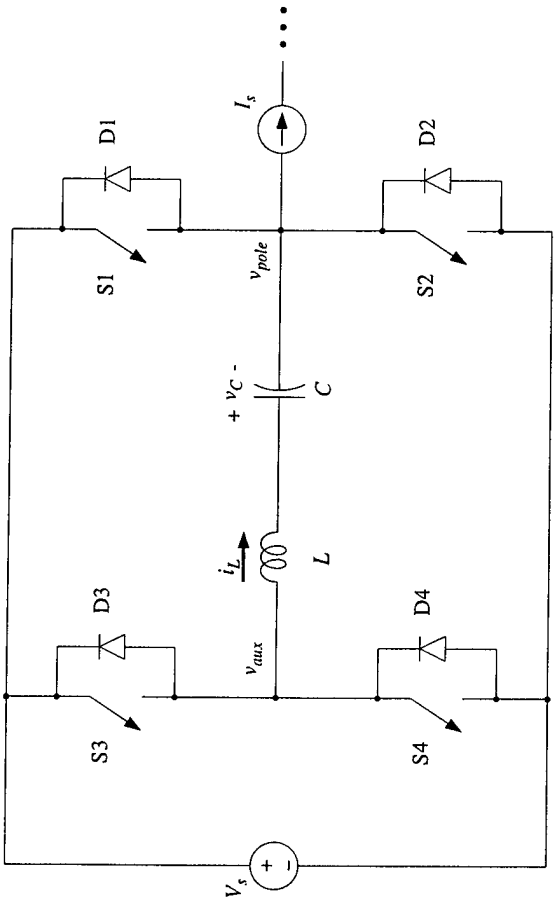

Figure 4.1 SSM Basic Circuit

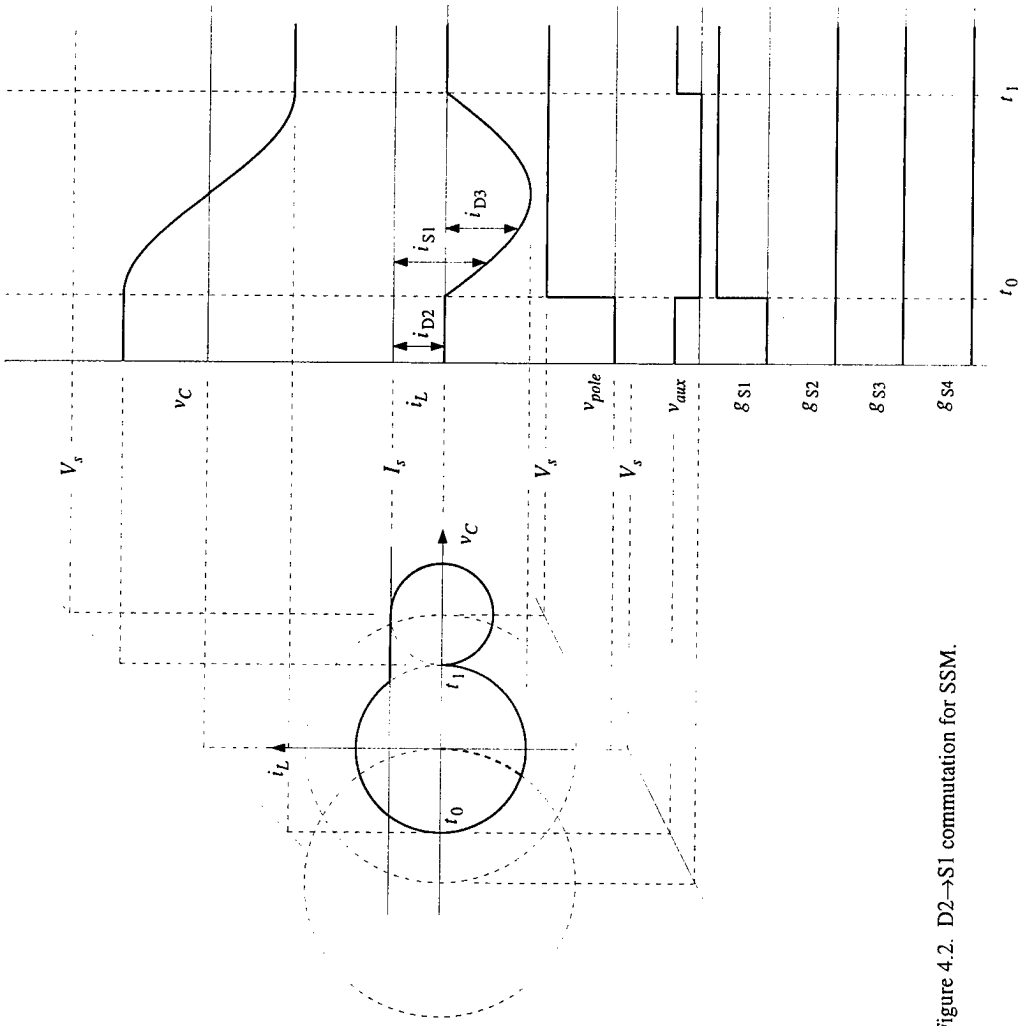

Figure 4.2. D2→S1 commutation for SSM.

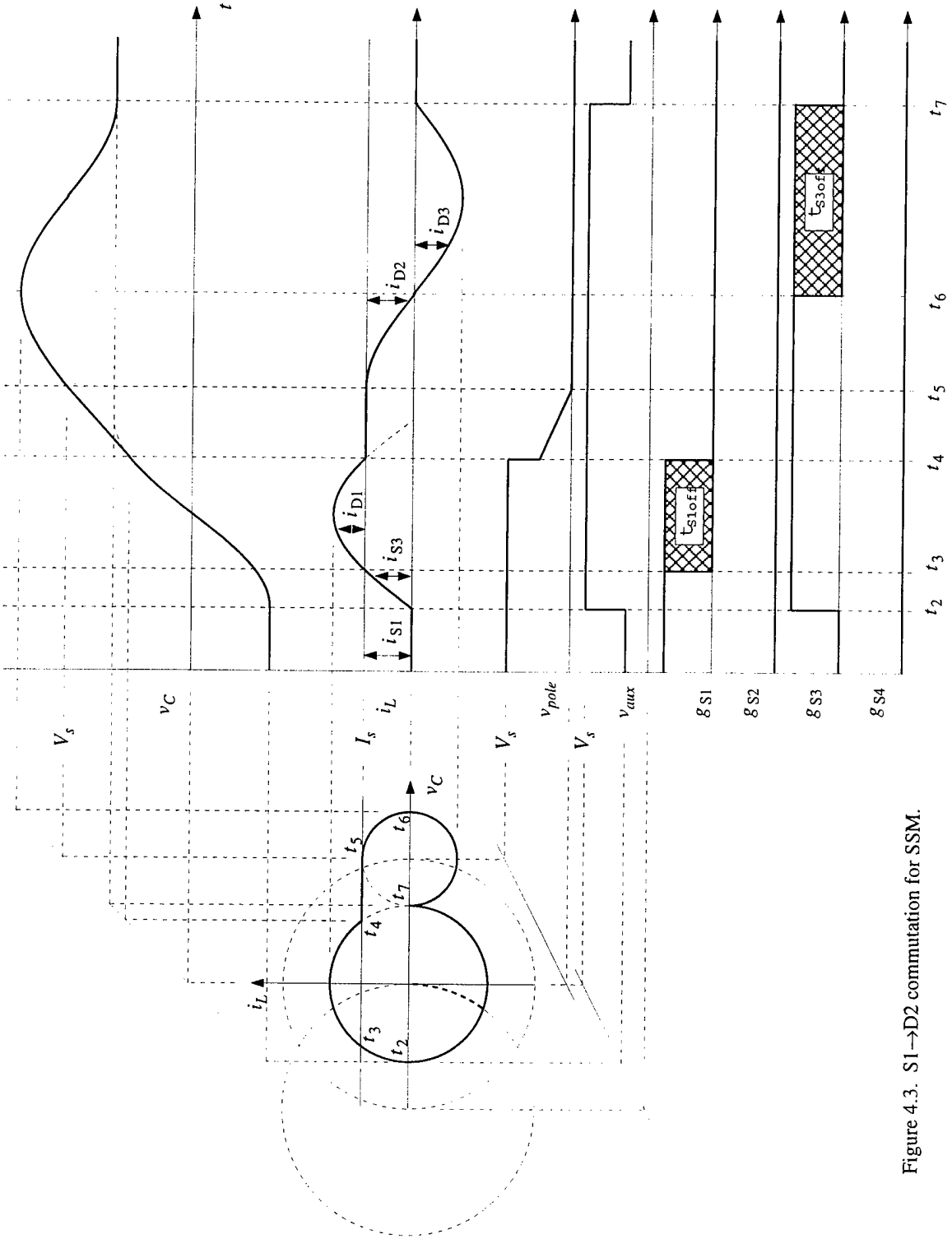

Figure 4.3. S1→D2 commutation for SSM.

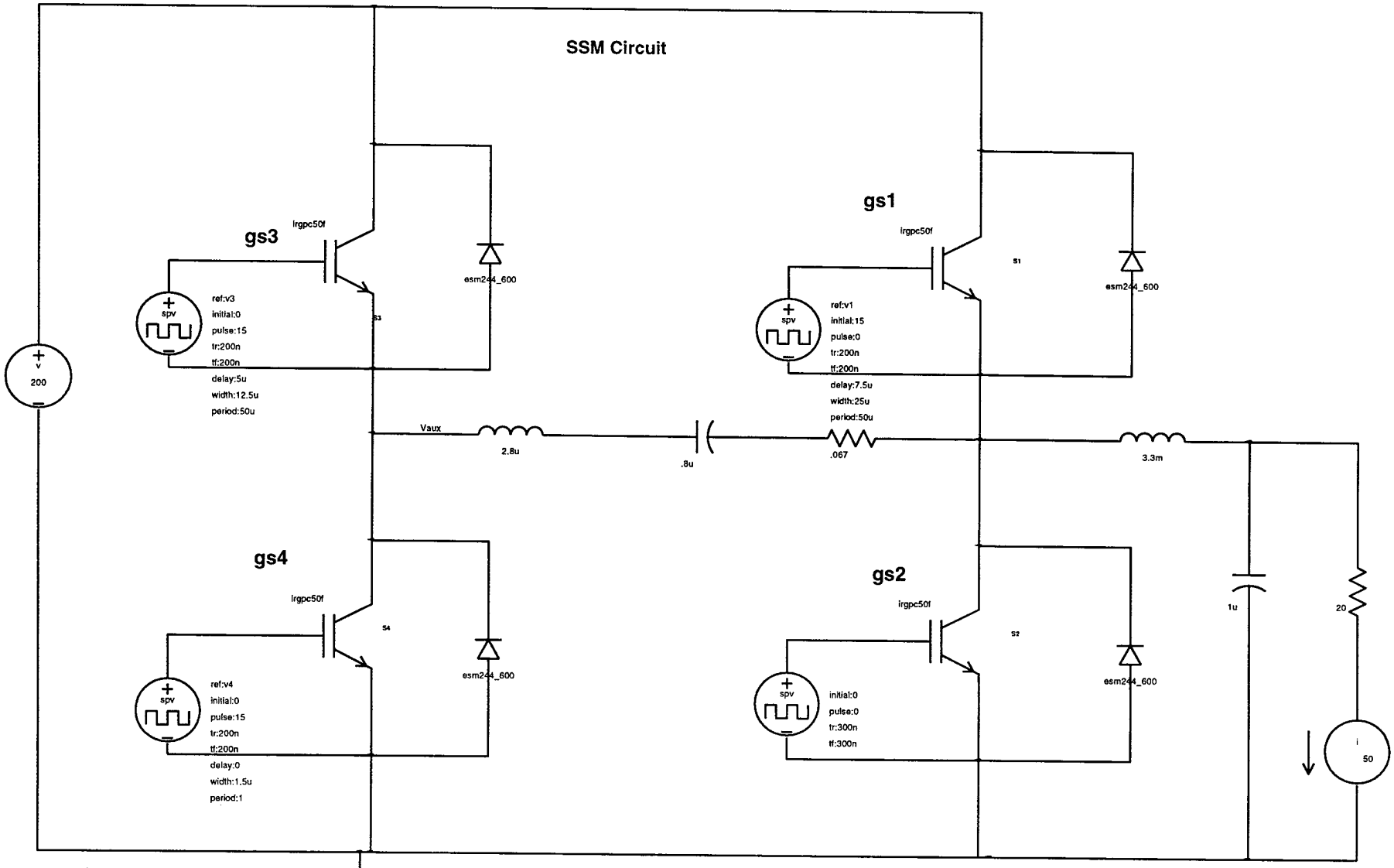

Figure 4.4 SSM Circuit

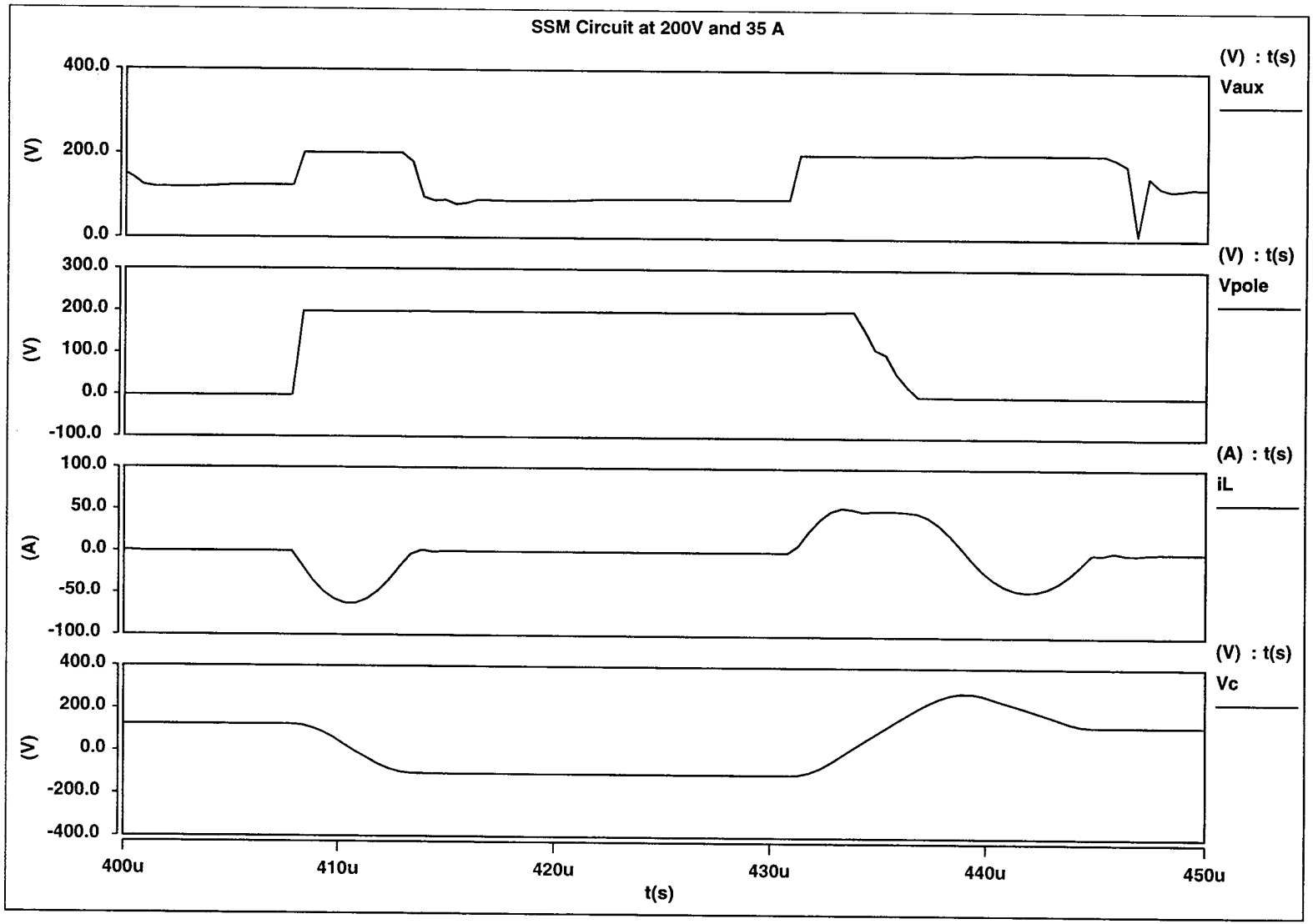

Figure 4.5 SSM Circuit Resonant Waveforms

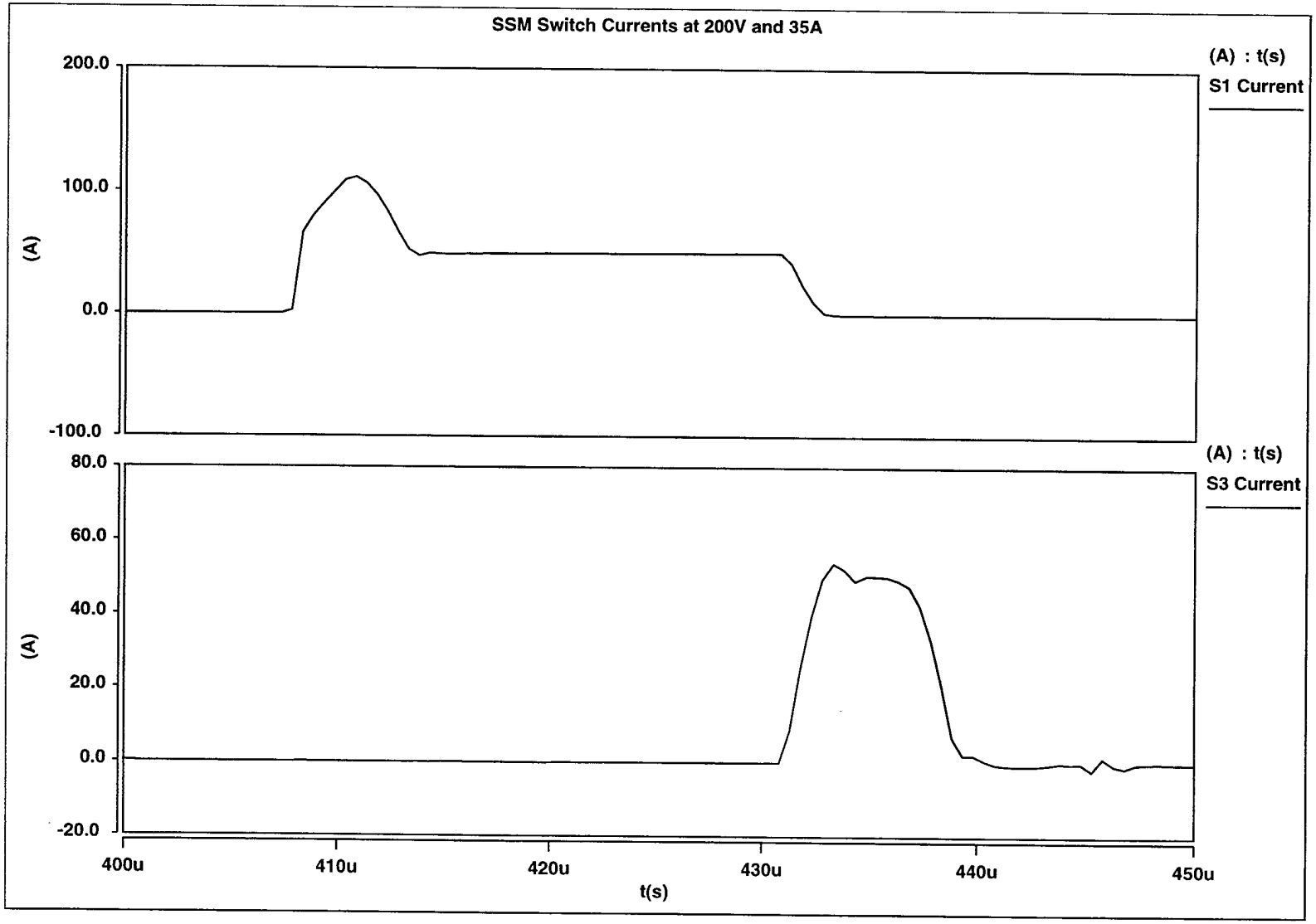

Figure 4.6 SSM Switch Currents

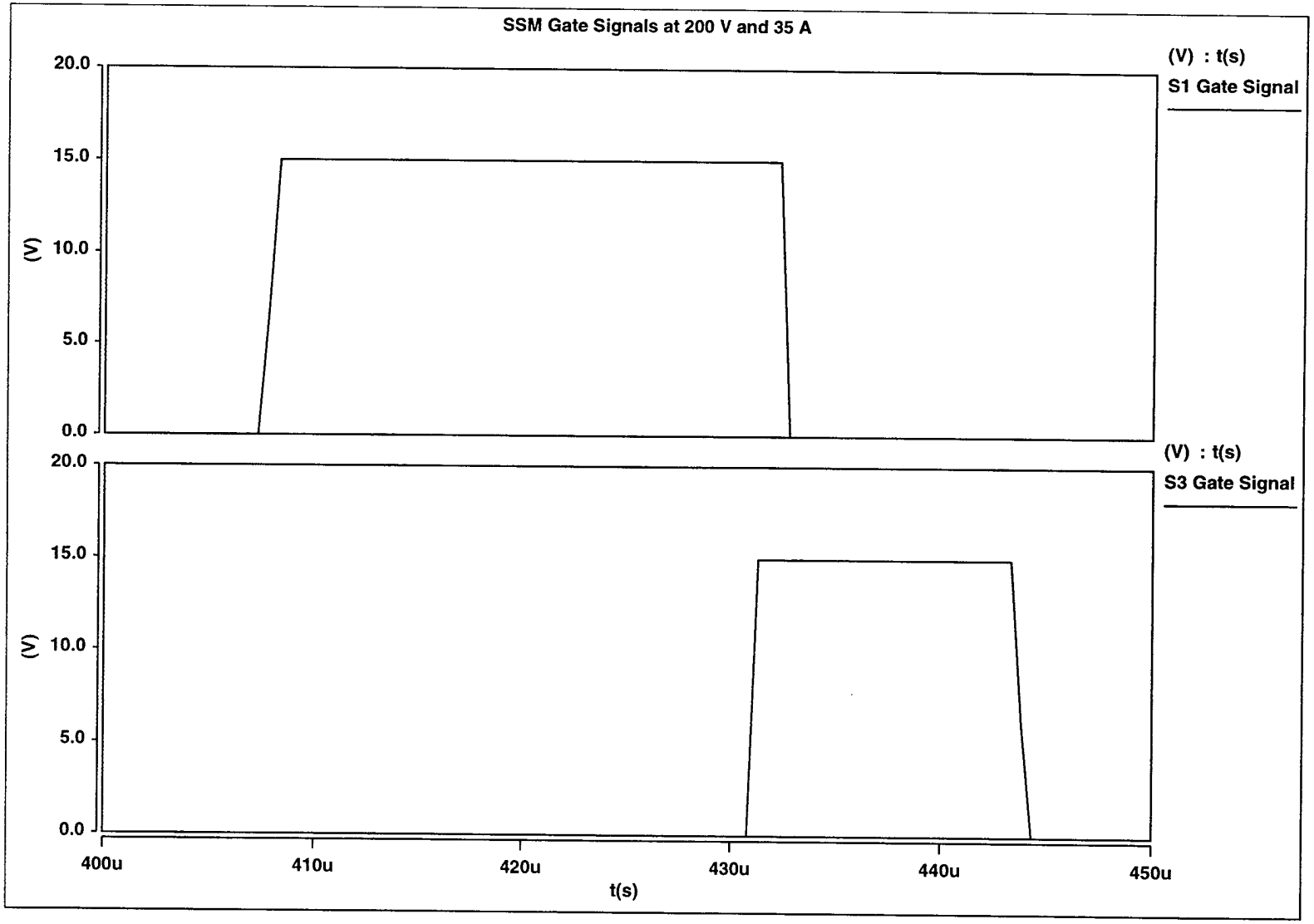

Figure 4.7 SSM Switch Timing

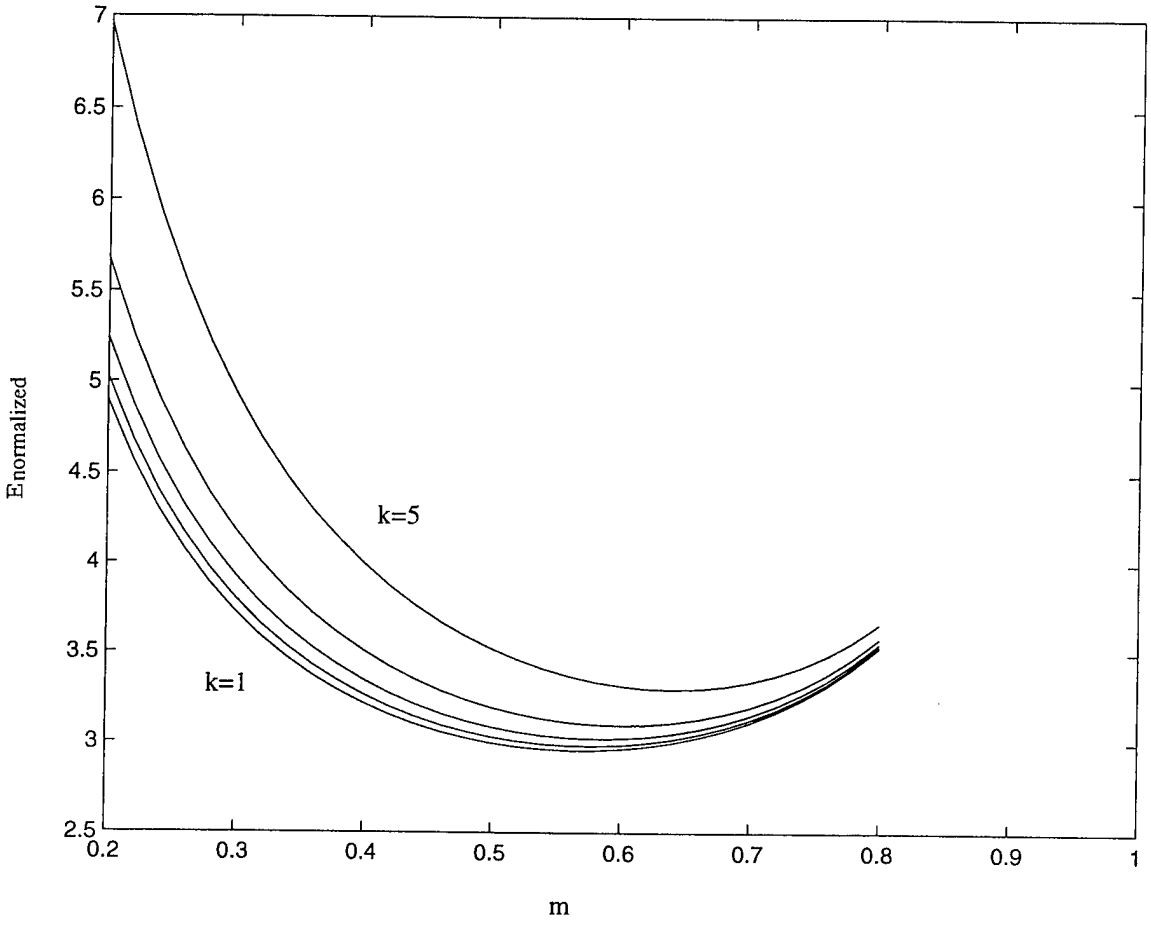

Figure 4.8 Plot of Enormalized vs. m

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CHAPTER 5
PEBB1 SWITCH TOPOLOGY WITH ZERO-CURRENT TURN OFF AND ADJUSTABLE-CURRENT TURN ON

5.1 INTRODUCTION

In this chapter, a converter switch topology that is similar to the ARCP or classic ac-switched modified McMurray is described. This topology can provide zero-current turn off and adjustable-current turn on so that switching losses can be minimized and the main diodes are not over stressed. The similarity to the ARCP can be seen in Fig. 5.1, which shows the topology. The primary difference between this topology for zero-current switching and the ARCP for zero-voltage switching is the lack of snubber capacitors across the main switches. In fact, it is the bank capacitors that have been eliminated; the capacitors shown in the figure are the resonant capacitors. The advantages of sharing the ARCP switch topology and permitting adjustable-current turn on as well as zero-current turn off are countered somewhat by significant turn-around time of approximately 2.5 times the resonant period (2.5 T_o).

Although this topology/strategy matches closely that of the classic ACSMM, a degree of freedom that is not utilized normally in the control of a classic thyristor-based design would be utilized for an MCT-based design to accommodate the severe mismatch between the *di/dt* ratings of the pole MCTs and the pole diodes. In particular, the desirable property of being able to utilize relative-time switching control to maintain a stable (and nearly minimum) value for the peak capacitor voltage is retained. To this is added the ability to control the magnitude of current commutated from a pole diode to the opposite MCT.

5.2 WAVEFORM ANALYSIS

Waveform analysis of the converter shown in Fig. 5.1 is complicated by the fact that the resonant "capacitance" is actually associated with the combination of the upper and lower capacitors. A circuit that is more readily analyzed can be obtained by applying

a Thevenin transformation looking into the capacitor pole from the auxiliary inductor. This yields the circuit shown in Fig. 5.2. Note that as long as the value of the capacitor in this new circuit is C = C_{upper}||C_{lower} the dynamics of the two circuits will be identical. The capacitor voltage v_C, resonant inductor current i_L, and the pole voltage v_{pole} waveforms along with the gating signals for the circuit in Fig. 5-2 are shown in Figs. 5.3 and 5.4. There are 20 instances of interest in these waveforms: t_0 through t_{10}, t_{S3on1}, t_{S1on}, t_{S3off1}, t_{S4off}, t_{S3on2}, t_{S1off}, t_{S2on}, t_{S2off}, and t_{S3off2}.

t_0: Initiation of the D2→S1 commutation

Commutation of the load current I_s, from D2 to S1 commences at t_0 with the gating on of S4. This results in a negative resonant inductor current pulse i_L, as the inductor is in a loop that also includes C, D2, D3, and S4; and the capacitor voltage v_C is initially $-V_s$.

t_{S3on1}: First controlled turn on of S3

As the negative inductor current is conducted by D3, S3 can be gated on without stress any time during the half resonant period between t_0 and t_1.

t_1: Natural S4→S3 commutation

With both S3 and S4 on, when i_L crosses zero going positive, it commutates from S4 and D3 to S3 and D4. Note also that i_L is increasing and the current through D2 is decreasing, which implies that S1 can be turned on with less than full-load current I_s.

t_2: Controlled turn on of S1

Switch S1 is turned-on t_2. This results in a negative swing of i_L. A key point to note is that the amount of load current to be picked up by S1 can be selected, with the caveat that lower current leads to greater energy trapped in the tank and thus greater peak capacitor voltage at t_4.

t_3: Natural S3→S4 commutation

As i_L passes through zero going negative, it commutates from S3 and D4 to S4 and D3. This allows for zero-current turn-off of S3.

t_{S3off1}: First controlled turn-off of S3

With i_L carried by S4, S3 can be turned off under no stress. Note the significant flexibility in turning off S3.

t_4: Return of i_L to zero and completion of D2→S1 commutation

After a half resonant pulse, i_L returns to zero and the resonant capacitor is fully charged to a value slightly greater than the input voltage V_s.

t_{S4off}: Controlled turn off of S4

With i_L restored to zero, S4 can be turned off at a convenient time. The intended duty cycle places an upper limit on this time.

t_5: Initiation of S1→D2 commutation

With the resonant capacitors fully charged and zero inductor current, S3 can be turned on under no stress to allow for a positive inductor current through S3.

t_6: Natural S1→D1 commutation

When i_L exceeds I_s, their difference commutates from S1 to D1.

t_{S1off}: Controlled turn off of S1

With I_s supplied by the resonant inductor, S1 can be turned off with zero current.

t_7: Natural turn off of D1

Diode D1 turns off naturally at t_7, as i_L drops to I_s. The inductor current remains frozen at I_s, because D2 remains reverse biased, as $v_C > -½V_s$ so $v_{pole} > 0$.

t_8: Controlled turn on of S2

With load current maintained for a brief interval, S2 can be turned on with zero current and low voltage. This provides a current path to remove the remaining charge from the resonant capacitor and to complete the resonant pulse so S3 can be turned off.

t_9: Natural S2→D2 commutation

Once I_s exceeds i_L, their difference commutates from S2 to D2.

t_{10}: Return of i_L to zero and completion of S1→D2 commutation

With the current path via S2, i_L returns to zero and the resonant capacitor voltage attains its initial value of $-V_s$.

5.3 Concept Simulation

Concept simulations of this topology and strategy have been performed to validate the previous analysis and to provide a basis for more detailed simulations to be used in design. A schematic of the circuit entered in Saber is shown in Fig. 5.5. This circuit is the

original circuit of Fig. 5.1, thus, when comparing the simulation analysis to the simulation results, the change in V_s and V_c must be taken into account. Each switch in this simulation is modeled as an IRGPC50F IGBT, which has voltage and current ratings of 600 V and 280 A, respectively. The tail interval is programmed to be approximately 270 ns, which is similar to the tail interval observed in the MCT models provided by Harris. The diode is modeled as an ESM 244_600, which has voltage and current ratings of 600V and 800A, respectively. This diode is particularly useful due to its relatively rapid reverse recovery characteristics and reverse recovery current limit of 6 A, which are representative of diodes that are likely to be used in an implementation. The voltage source and current source are simple dc sources without ac noise. The capacitors and inductors are also basic devices with initial conditions set to zero. All resistor components are set to the indicated values without thermal effects being simulated. The output inductor is set to an initial value of steady-state load current and the resonant capacitors are set to an initial value of voltage as discussed in Section 5.2.

The converter was simulated under a variety of load conditions ranging from I_s = 20 A to I_s = 150 A. Operation at I_s = 50 is depicted in Figs. 5.6-5.8, which shows the pole voltage v_{pole}, the resonant inductor current i_L, the upper resonant capacitor voltage v_{upper}, and the lower resonant capacitor voltage v_{lower}. To facilitate comparison between these simulation waveforms and the previous analysis, the simulation time of several of the key instants are listed in Table 5.1. The overall similarity between these waveforms and those in Figs. 5.3 and 5.4 indicates that the analysis is correct. The switch currents S1 and S4 attain peak current values equivalent to approximately 2.5 times load current. The recovery effects of diodes during S1 turn off and S4 turn off are seen in the simulation, but do not cause any stress issues.

The resonant inductor current at time t_8 attains a slightly lower value during it S2 commutation due to following a slightly smaller trajectory on the state-plane plot. Additionally, the time interval of constant i_L does not exist due to the slightly earlier turn on of S2. The simulation shows that this does not cause any additional stress across S2 during turn on.

Table 5.1 Comparison of Simulation Time to Analysis Time

Analysis Instant	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9

Simulation Time (μs)	30	36	38	39	55	58	59	62	63	65

5.4 Control Synthesis

A robust control method that detects resonant inductor current utilizing one of the methods discussed in Appendix B could be implemented with this topology. One of the most critical instances is the turn on of S1 at t_2 of Fig. 5.3. This point effects both the turn-on (turn-off) stress of S1 (D2) and the peak value of v_C. Due to the importance of t_2 and its distance from t_0, a pure relative time control seems to be inappropriate. Instead, t_2 should be determined relative to t_1, which corresponds to the zero crossing of i_L. This zero crossing can be detected readily using one of the techniques described in Appendix B. The precise resonant period can then be determined and the turn on of S1 can occur with appropriate time delays that are determined based on the resonant period.

A second critical instant is the turn on of S2 at t_8. As with t_2, this instant effects the peak value of V_c. Since S2 is determined mathematically, it can be programmed as a function of the resonant period once the resonant period is determined as in the case with S1 turn on. Determination of S2 turn on time is discussed in greater detail in the following section.

5.5 Design Optimization and Trade-Offs

Design optimization for the ACSMM is similar to that for the MLZDCB and SSM described in Chapters 2 and 4, respectively. The additional degree of freedom used to limit the turn-off stress of the diodes does result, however, in a slightly more complicated expression for the additional losses arising from use of the auxiliary circuit.

In the analysis described in Section 5.2, specific values for the resonant inductor L and capacitor C were not necessary, as a normalized state-plane was employed. In the design of a practical converter, however, the selection of L and C is critically important to obtain "optimal" converter performance and avoid excessive component stress. The selection of L and C is done best by a process in which "optimal" converter performance is defined explicitly (mathematically).

Ultimately, the process of selecting L and C ($\frac{1}{2}C_{upper}$ and $\frac{1}{2}C_{lower}$) will require identifying the maximum dc input voltage V_s and the maximum (instantaneous) ac output current I_s specifications for the converter as well as the circuit-commutated turn-off time t_q

of the main and auxiliary switches and the maximum allowable hard-switched current. These values then represent design parameters. Within the process, it is assumed there are two primary criteria for optimal performance of the converter. The first is related to t_q of the main switches. In particular, the window in which to turn off S1 under zero current must be greater than t_q by up to a factor of two, depending upon the gating control method (see previous section). This criterion is necessary to avoid inadvertent turn on of a main switch and will lead to a mathematical relationship between the resonant period T_o, which is related to L and C, ($T_o = 2\pi(LC)^{1/2}$) and the ratio of the output current I_s to the peak resonant inductor current $I_{L,peak}$; this ratio is a key design variable and will be referred to as m. The second criterion is that the additional conduction losses in the auxiliary and main switches due to the resonant current pulses should be minimal. This criterion will be met explicitly by minimizing a mathematical expression for the additional losses with respect to the design variable $m = I_s/I_{L,peak}$. The design process will now be described.

The starting point is determining the relationship between T_o and $m = I_s/I_{L,peak}$, given the constraint $T_{S1off} = t_7 - t_6 \geq t_q$. The boundaries of the T_{S1off} window are the intersections of the constant output current with the resonant inductor current pulse. These intersections can be expressed

$$I_s = I_{L,peak}\cos\left(\frac{2\pi t}{T_o}\right) \qquad 5.5\text{-}1$$

where it is assumed that the time reference is midway between t_3 and t_4. Solving for t

$$t = \frac{T_o}{2\pi}\cos^{-1}\left(\frac{I_s}{I_{L,peak}}\right) \qquad 5.5\text{-}2$$

This implies that

$$T_{off} = t_4 - t_3 = \frac{T_o}{\pi}\cos^{-1}\left(\frac{I_s}{I_{L,peak}}\right) \qquad 5.5\text{-}3$$

Denoting the ratio of I_s to $I_{L,peak}$ as m

$$T_{off} = \frac{T_0}{\pi}\cos^{-1} m \qquad 5.5\text{-}4$$

Ultimately, T_{off} will be set based on the design parameter t_q, and m will be selected through

an optimization (minimization) process, so this equation will provide the desired resonant frequency that, in turn, will provide L and C.

Although the resonant circuit is used to reduce switching losses of the pole switches, its resonant current pulses will result in new losses in the auxiliary circuit and greater conduction losses in the main switches. Intuitively, the magnitude of the additional losses will be related to the magnitude of the resonant current pulses, which can be expressed in terms of the design parameter I_s and design variable m (i.e., I_s/m). The exact expression for the additional losses can be derived in two parts. First the new losses will be expressed for the auxiliary circuit, which includes an auxiliary switch (corresponding to either the controlled device or the diode), the resonant inductor, and resonant capacitor. Second, the conduction losses in excess of the "hard-switched" conduction losses of the main switches will be expressed. In both cases, it assumed that the conduction losses can be expressed as the product of a constant voltage drop times an appropriate current. This constant-voltage model is much simpler to work with than a more realistic one that includes a constant on-state voltage for the switch plus an ohmic term Ri_L for the passive components. More accurate modeling is probably done better using a circuit simulation program. In any event, the auxiliary circuit voltage drop will be denoted V_c. The drop for the main switches will be denoted as V_c/k, where k typically lies between 2 and 4, as the "equivalent power" loss in the auxiliary circuit passive components corresponds to between ½ and ¾ of the auxiliary circuit losses.

The auxiliary circuit losses can now be expressed

$$E_{aux} = \int_{t_0}^{t_4} V_c |i_L| dt + \int_{t_5}^{t_{10}} V_c |i_L| dt \qquad 5.5\text{-}5$$

$$= V_c \left[\int_{t_0}^{t_1} -i_L dt + \int_{t_1}^{t_3} i_L dt + \int_{t_3}^{t_4} -i_L dt + \int_{t_5}^{t_{10}} i_L dt \right] \qquad 5.5\text{-}6$$

Because i_L flows through the resonant capacitor, the various integrals of i_L in this expression can be related to the capacitor voltages at the bounds of integration

$$E_{aux} = V_c \begin{bmatrix} -v_C(t_1) + v_C(t_0) + v_C(t_3) - v_C(t_1) - v_C(t_3) - v_C(t_4) \\ + v_C(t_{10}) - v_C(t_5) \end{bmatrix} \qquad 5.5\text{-}7$$

This expression can be simplified by noting that $v_C(t_0) = - v_C(t_{10})$, $v_C(t_5) = v_C(t_4)$, and

$v_C(t_1) = 0$

$$E_{aux} = 2V_c C[v_C(t_{10}) + v_C(t_3) - v_C(t_4)] \qquad 5.5\text{-}8$$

To get back to an expression in terms of design parameters, note that $v_C(t_{10})$ corresponds to $-V_s$, while the difference $v_C(t_3) - v_C(t_4)$ corresponds to the diameter of the right orbit, which can also be expressed $2(L/C)^{1/2} I_{L,peak}$. Thus,

$$E_{aux} = 2V_c C\left[V_s + \sqrt{L/C}\, I_{L,peak}\right] \qquad 5.5\text{-}9$$

The V_s term can be eliminated from this expression by noting that it too is actually related to $I_{L,peak}$. In particular, the square of the radius of the right-hand orbit can be expressed as

$$\left[\tfrac{1}{2}\sqrt{C}V_s + (1-\cos\beta)\tfrac{1}{2}\sqrt{C}V_s\right]^2 + \left(\tfrac{1}{2}\sqrt{C}V_s \sin\beta\right)^2 = \left(\sqrt{L} I_{L,peak}\right)^2 \qquad 5.5\text{-}10$$

where $\beta = \omega_o(t_2 - t_1)$ is a controlled delay used to limit the current commutated from a main diode to a main MCT. This equation can be simplified to

$$V_s = 2\sqrt{\frac{L}{C}}(5 - 4\cos\beta)^{-1/2} I_{L,peak} \qquad 5.5\text{-}11$$

Substituting this in to (5.5-11) yields

$$E_{aux} = 4\sqrt{LC}\left[(5 - 4\cos\beta)^{-1/2} + 1\right] V_c I_{L,peak} \qquad 5.5\text{-}12$$

$$E_{aux} = \frac{2}{\pi}\left[(5 - 4\cos\beta)^{-1/2} + 1\right] V_c I_{L,peak} T_o \qquad 5.5\text{-}13$$

The additional main switch losses occur when these devices carry resonant current with magnitude exceeding the magnitude of the output current. This occurs between t_6 and t_7 and between t_8 and t_9 as well as the corresponding intervals in the other half of the state-plane orbits. For every other time during a resonant cycle, an increase (decrease) in main switch current is countered by a decrease (increase) at another time. The additional conduction losses in the main switches can be expressed

$$E_{main} = 2\int_{t_3}^{t_4} \frac{V_c}{k}\left[I_{L,peak}\cos\omega t - I_s\right] dt \qquad 5.5\text{-}14$$

$$E_{main} = 2\left[\int_{t_6}^{t_7} \frac{V_c}{k}(i_L - I_s)dt + \int_{t_8}^{t_9} \frac{V_c}{k}(i_L - I_s)dt\right] \qquad 5.5\text{-}15$$

The first integral is of exactly the same form as seen previously for the MLZDCB and SSM. The second integral is associated with the second resonant pulse (left-hand orbit). Because the first integral is similar in form to that for the MLZDCB and SSM, it can be simplified immediately. Simplification of the second integral is shown here

$$E_{main} = 2\frac{V_c}{k}\left[\int_{t_6}^{t_7}\left(I_{L,peak}\cos\omega t - I_s\right)dt + \int_{t_8}^{t_9}\left(\sqrt{\frac{C}{L}}\frac{V_s}{2}\cos\omega t - mI_{L,peak}\right)dt\right] \qquad 5.5\text{-}16$$

$$= \frac{2}{\pi}\left(\sqrt{1-m^2} - m\cos^{-1}m\right)\frac{V_c}{k}I_{L,peak}T_0 + 2\frac{V_c}{k}\frac{1}{\omega}\sqrt{\frac{C}{L}}\frac{V_s}{2}\left(\sin\omega t\,\Big|_{t_8}^{t_9} - mI_{L,peak}t\Big|_{t_8}^{t_9}\right)$$

5.5-17

$$= \frac{2}{\pi}\left(\sqrt{1-m^2} - m\cos^{-1}m\right)\frac{V_c}{k}I_{L,peak}T_0 + 2\frac{V_c}{k}\left[2\frac{1}{\omega}\sqrt{\frac{C}{L}}\frac{V_s}{2}\sqrt{\frac{CV_s^2 - 4LI_s^2}{CV_s^2}} - mI_{L,peak}2\frac{1}{\omega}\cos^{-1}\left(\sqrt{\frac{L}{C}}2\frac{I_s}{V_s}\right)\right] \qquad 5.5\text{-}18$$

$$= \frac{2}{\pi}\left(\sqrt{1-m^2} - m\cos^{-1}m\right)\frac{V_c}{k}I_{L,peak}T_0 + \frac{2}{\pi}\left[\frac{1}{2}\sqrt{\frac{C}{L}V_s^2 - 4I_s^2} - mI_{L,peak}\cos^{-1}\left(\sqrt{\frac{L}{C}}2\frac{I_s}{V_s}\right)\right]\frac{V_c}{k}T_0 \qquad 5.5\text{-}19$$

$$= \frac{2}{\pi}\left(\sqrt{1-m^2} - m\cos^{-1}m\right)\frac{V_c}{k}I_{L,peak}T_0 + \frac{2}{\pi}\left[\frac{1}{2}\sqrt{I^2_{L,peak}\left(5/4 - \cos\beta\right)^{-1} - 4m^2I^2_{L,peak}} - mI_{L,peak}\cos^{-1}\left(\sqrt{\frac{L}{C}}\frac{2mI_{L,peak}}{\sqrt{\frac{L}{C}}I_{L,peak}\left(5/4 - \cos\beta\right)^{-1/2}}\right)\right]\frac{V_C}{k}T_0$$

5.5-20

$$E_{main} = \frac{2}{\pi}\left[\sqrt{1-m^2} - m\cos^{-1}(m) + \sqrt{\frac{1}{5-4\cos\beta} - m^2} - m\cos^{-1}((5-4\cos\beta)m)\right]\frac{V_c}{k} I_{L,peak} T_o$$

5.5-21

Note that for the case where $\beta = 0$ (i.e., classic hard-switched ACSMM operation), the third and fourth terms match the first and second, so there is simply twice the energy dissipation. This is consistent with the fact that for the $\beta = 0$ case the two orbits have the same radius.

The total additional losses due to the use of auxiliary resonant circuit can be expressed as the sum of the two separate components.

$$E_{loss} = \left[\frac{2}{\pi}\left(\frac{\sqrt{1-m^2} - m\cos^{-1} m + \sqrt{\frac{1}{5-4\cos\beta} - m^2} - m\cos^{-1}((5-4\cos\beta)m)}{k} + 8\pi\left[(5-4\cos\beta)^{-1/2} + 1\right]\right)\right] T_0 V_c I_{L,peak}$$

5.5-22

Given I_s, T_{off}, and now V_c as design parameters, this expression can be normalized as

$$E_{normalized} = \frac{E_{loss}}{2V_c I_s T_{off}}$$

5.5-23

$$= \frac{\left(\frac{\sqrt{1-m^2} - m\cos^{-1} m + \sqrt{\frac{1}{5-4\cos\beta} - m^2} - m\cos^{-1}((5-4\cos\beta)m)}{k} + 4\pi^2\left[(5-4\cos\beta)^{-1/2} + 1\right]\right)}{m\cos^{-1} m}$$

5.5-24

This expression relates the additional losses due to the auxiliary circuit to the design variable m, the design parameter k, and the operating variable β. A family of plots of $E_{normalized}$ vs. m is shown in Fig. 5.9 for k ranging from 1 to 5 and β ranging from 0° to 60°. The truncated curves of Fig. 5.9 correspond to large values of β for which m is limited. From these plots, it can be deduced that the optimal value of M is in the interval [0.5,0.7]. The specific design value for m is denoted as M. Once M has been selected, the resonant period can be calculated.

$$T_o = \frac{\pi T_{off}}{\cos^{-1} M} \qquad 5.5\text{-}25$$

Because $T_o = 2\pi(LC)^{1/2}$, there is now one equation relating these to desired parameter values. A second equation comes from the relationship between $I_{L,peak}$ and V_s discussed previously. $I_{L,peak}$ in this equation can now be replaced by MI_s. The simultaneous solution of these two equations yields the following expressions for L and C

$$L = \frac{V_s T_{off}}{2MI_s \cos^{-1} M} \qquad 5.5\text{-}26$$

$$C = \frac{MT_{off} I_s}{2V_s \cos^{-1} M} \qquad 5.5\text{-}27$$

These formulas can be used to determine values for the resonant inductor and capacitor that can then be refined through simulation and/or experimentation.

The design optimization just described does not address the impact of turn-around time on converter performance, as the resonant period was determined based on minimizing auxiliary circuit losses. To avoid the deleterious effects of turn-around time on bus utilization and THD it may be necessary to accept additional losses. The actual losses will also be higher due to turn-on losses that have not been modeled.

This topology appears to offer a good compromise of reduced switch stress and optimal passive component rating. The switch stress is reduced from an ARCP-type topology by the zero-current turn off and instances of reduced-current turn on. Significant time flexibility of the gating signals for this topology is also an advantage that will simplify control. The key disadvantage of this topology is the relatively long turn-around time. Innovative techniques for initiating each commutation cycle can mitigate the negative effect of the turn-around time.

The optimal passive component rating of this topology is illustrated by the fact that the peak voltage of the resonant capacitors will not exceed V_s by more than a few percent regardless of the value of load current being supplied. This holds true as long as S2 is gated on approximately one half of the resonant period after S3 is gated off. As long as this relationship is maintained, the resonant capacitor rating is limited to V_s with a slight additional margin for overshoot do to slight variations from the one half cycle constraint that may occur due to control techniques.

Another key issue to consider in the implementation of this topology is that the *di/dt* and *dv/dt* stress applied to the MCTs. The simulation results indicate that the most severe *di/dt* instances occur during the second turn-off of S3 and the turn-on of S2. These values will be mitigated to a certain extent by the parasitic inductance that is inherent to the devices and the circuit. The *dv/dt* the devices are exposed to is a somewhat more difficult problem. At the turn-on of S2 a large *dv/dt* stress is applied to the device. Additionally, at turn-on and subsequent turn-off of S1 a voltage equivalent to V_s is applied to S1 yielding a *dv/dt* stress as well. Due to the devices chosen for implementation, the *dv/dt* stress does not appear to be a limiting factor in this topology.

5.6 Conclusions

The ACSMM appears to be a good candidate for a zero-current topology due to its lack of any trapped energy problems and its reduced switch stress when compared to other zero-current topologies. The apparent key limitation of this topology is its long turn-around time.

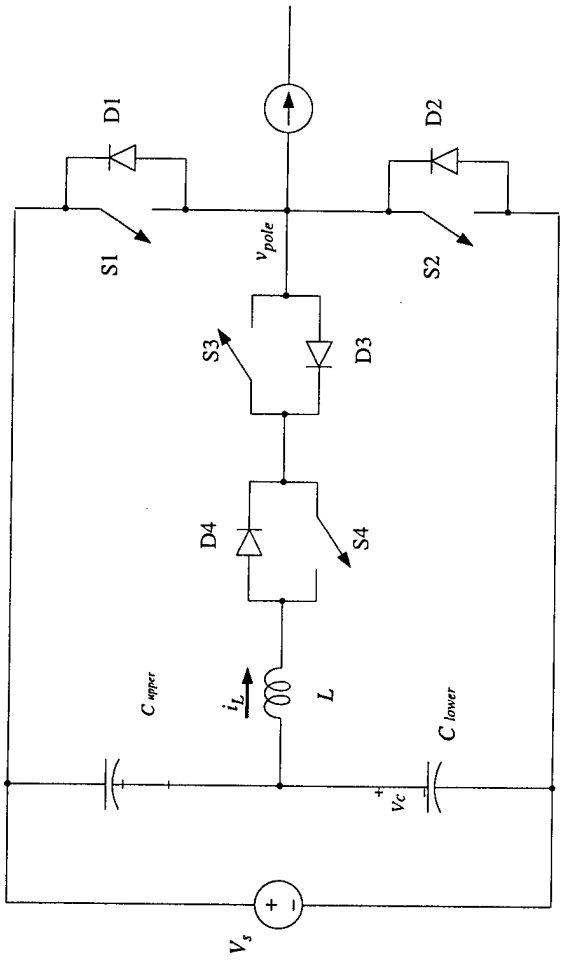

Figure 5.1. Schematic of ac-switched modified McMurray.

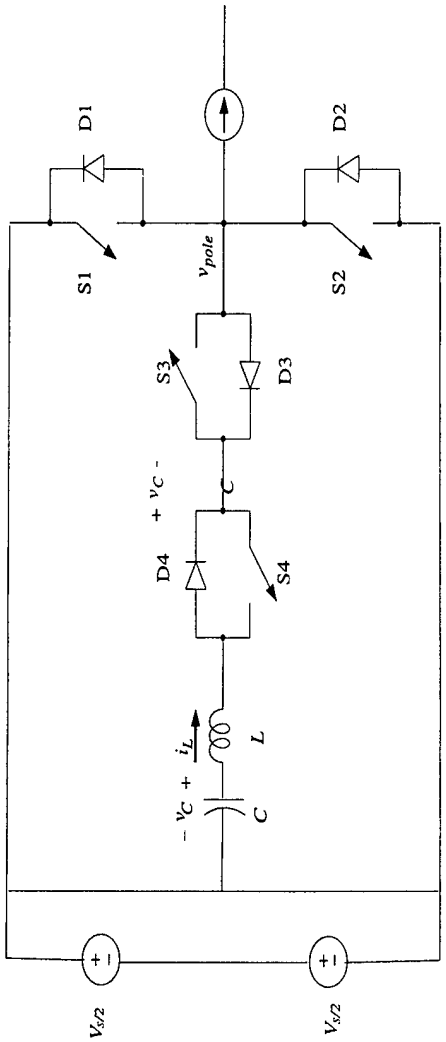

Figure 5.2. Schematic of ac-switched modified McMurray Thevenin-Equivalent Circuit

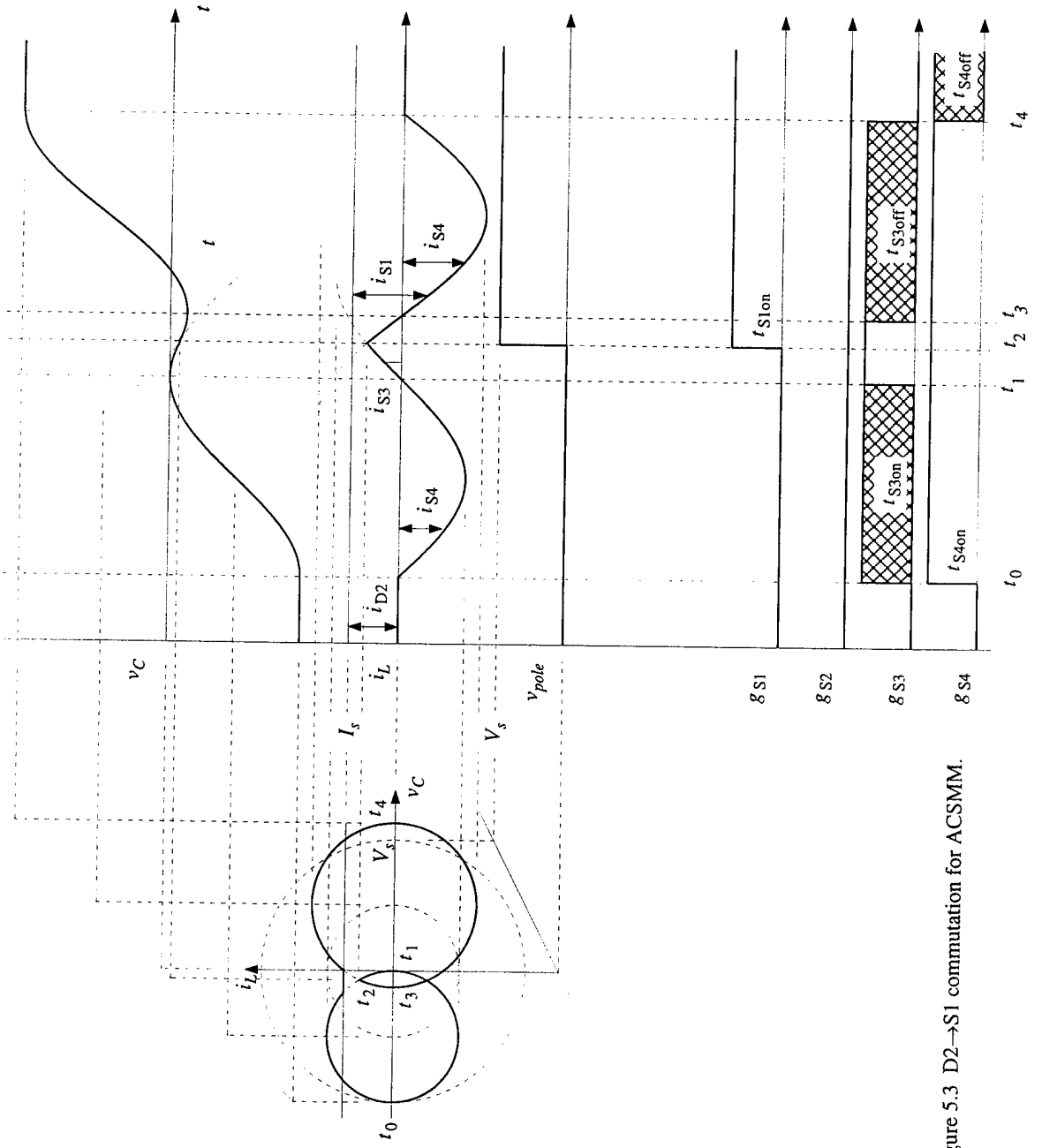

Figure 5.3 D2→S1 commutation for ACSMM.

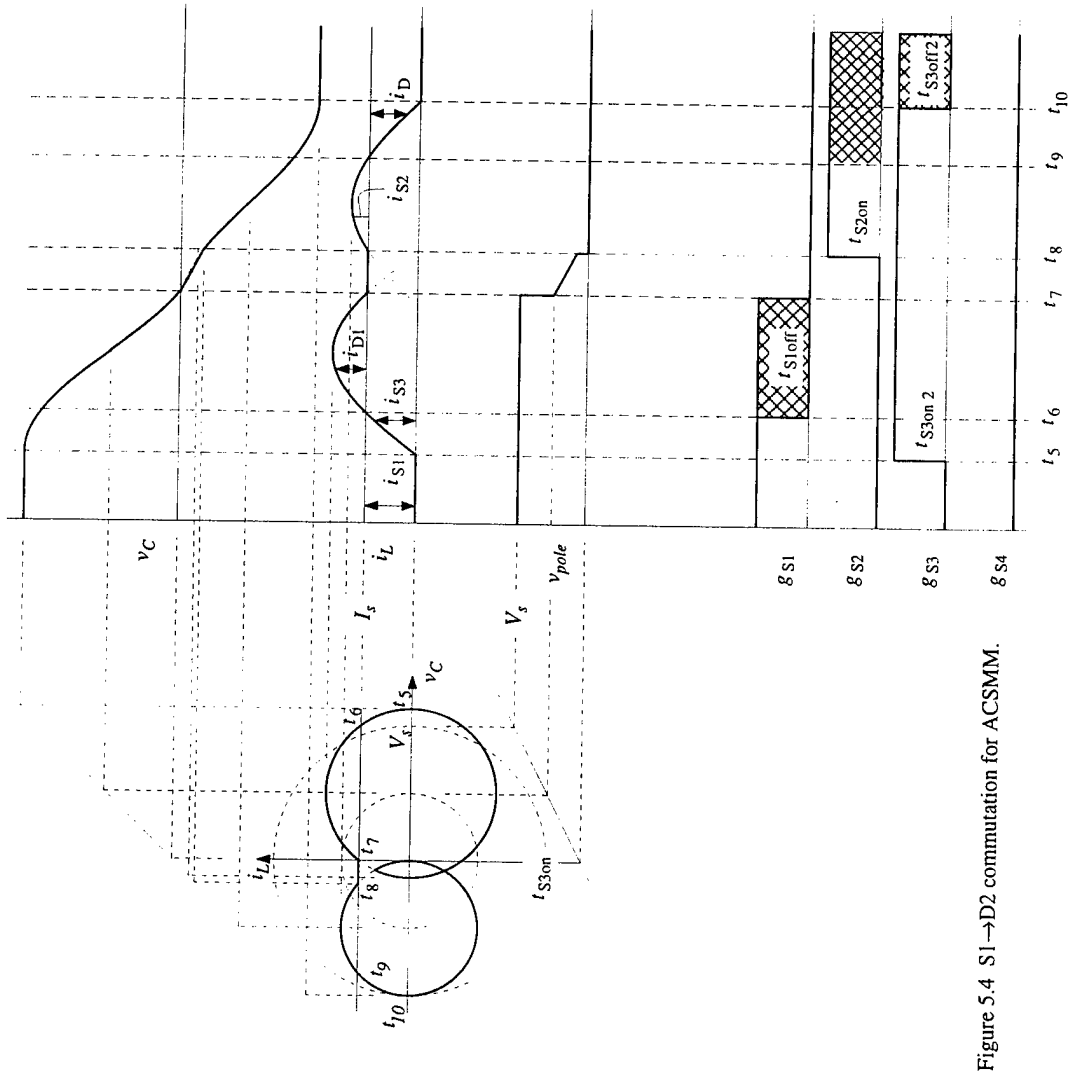

Figure 5.4 S1→D2 commutation for ACSMM.

ACSMM

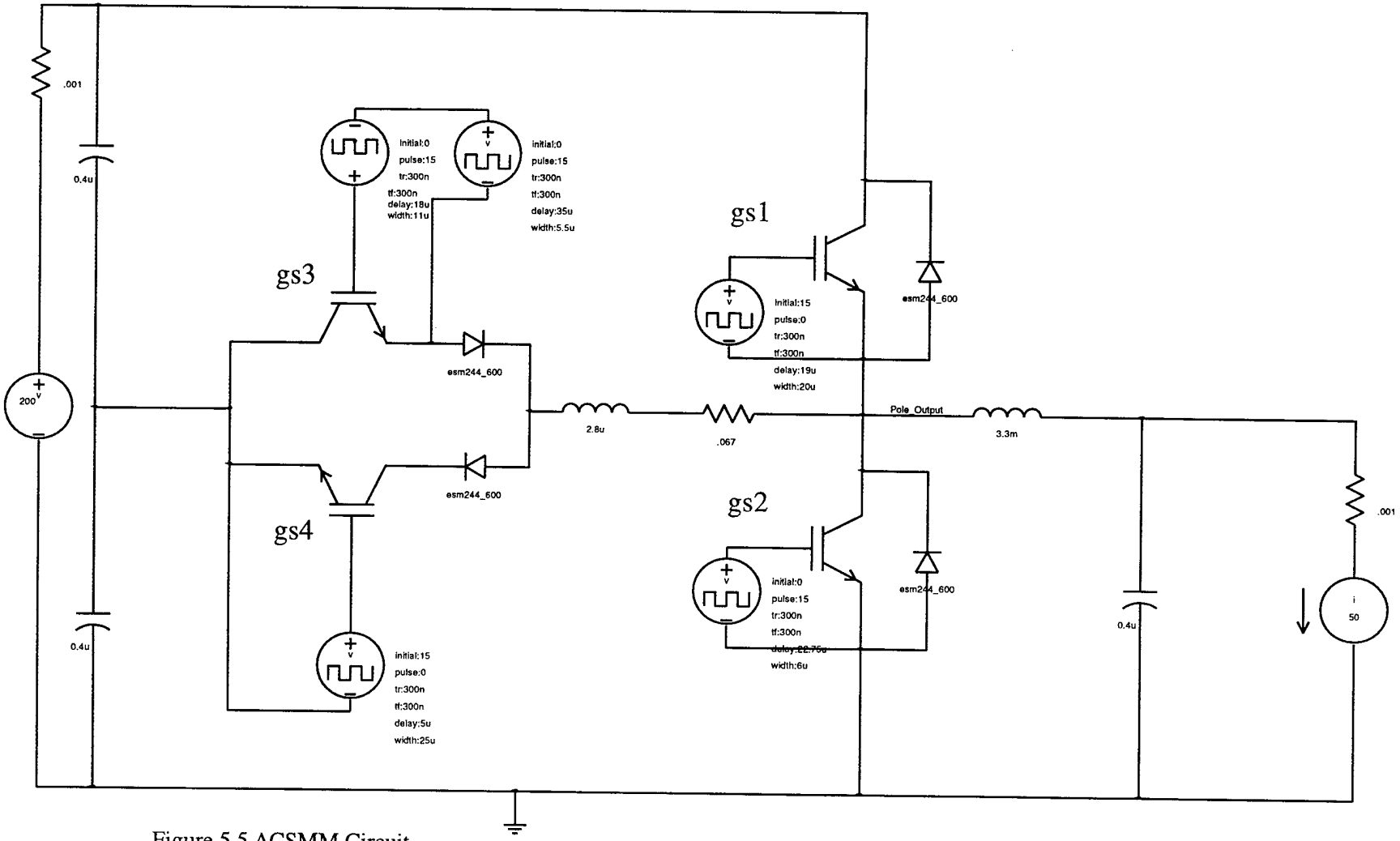

Figure 5.5 ACSMM Circuit

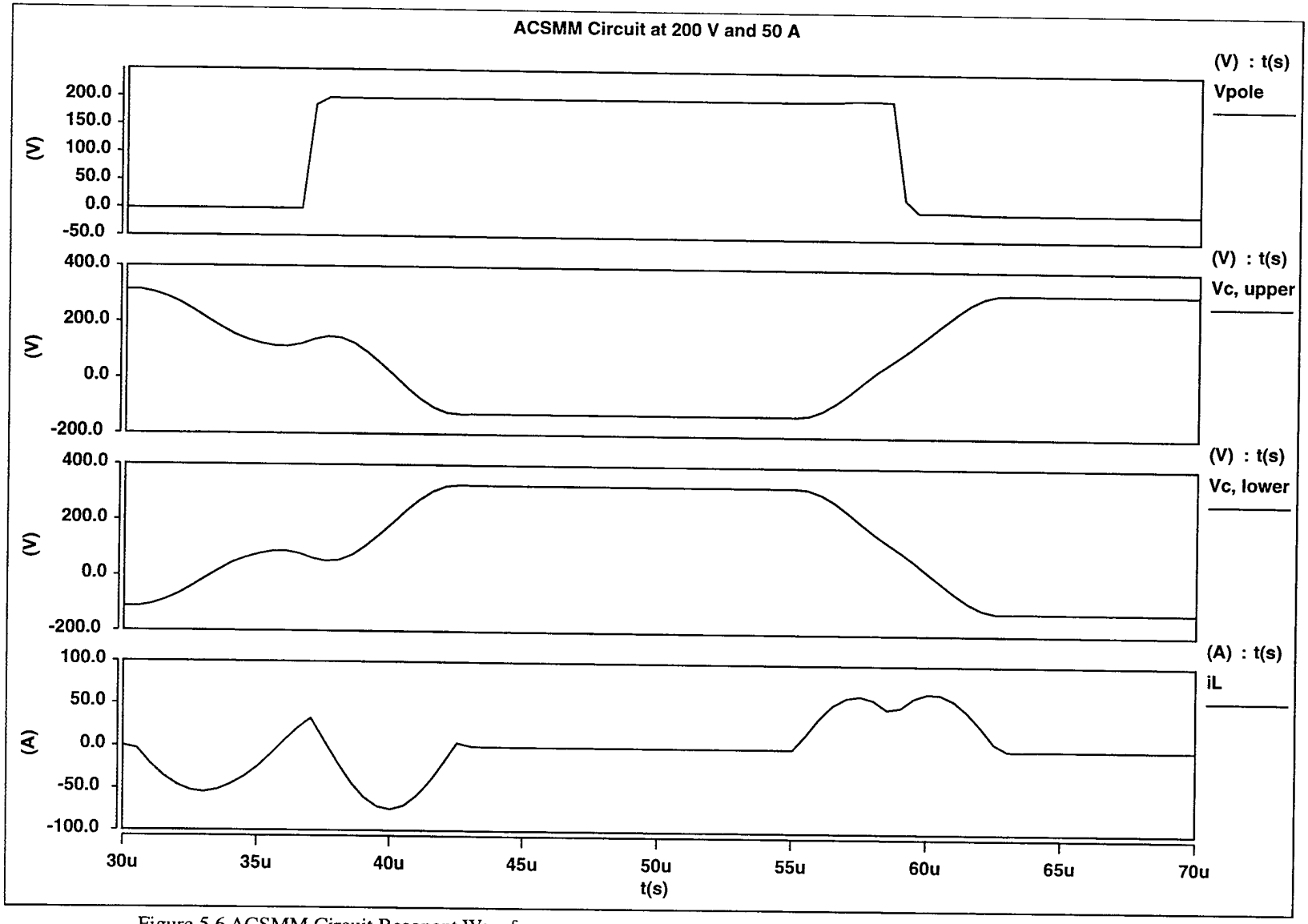

Figure 5.6 ACSMM Circuit Resonant Waveforms

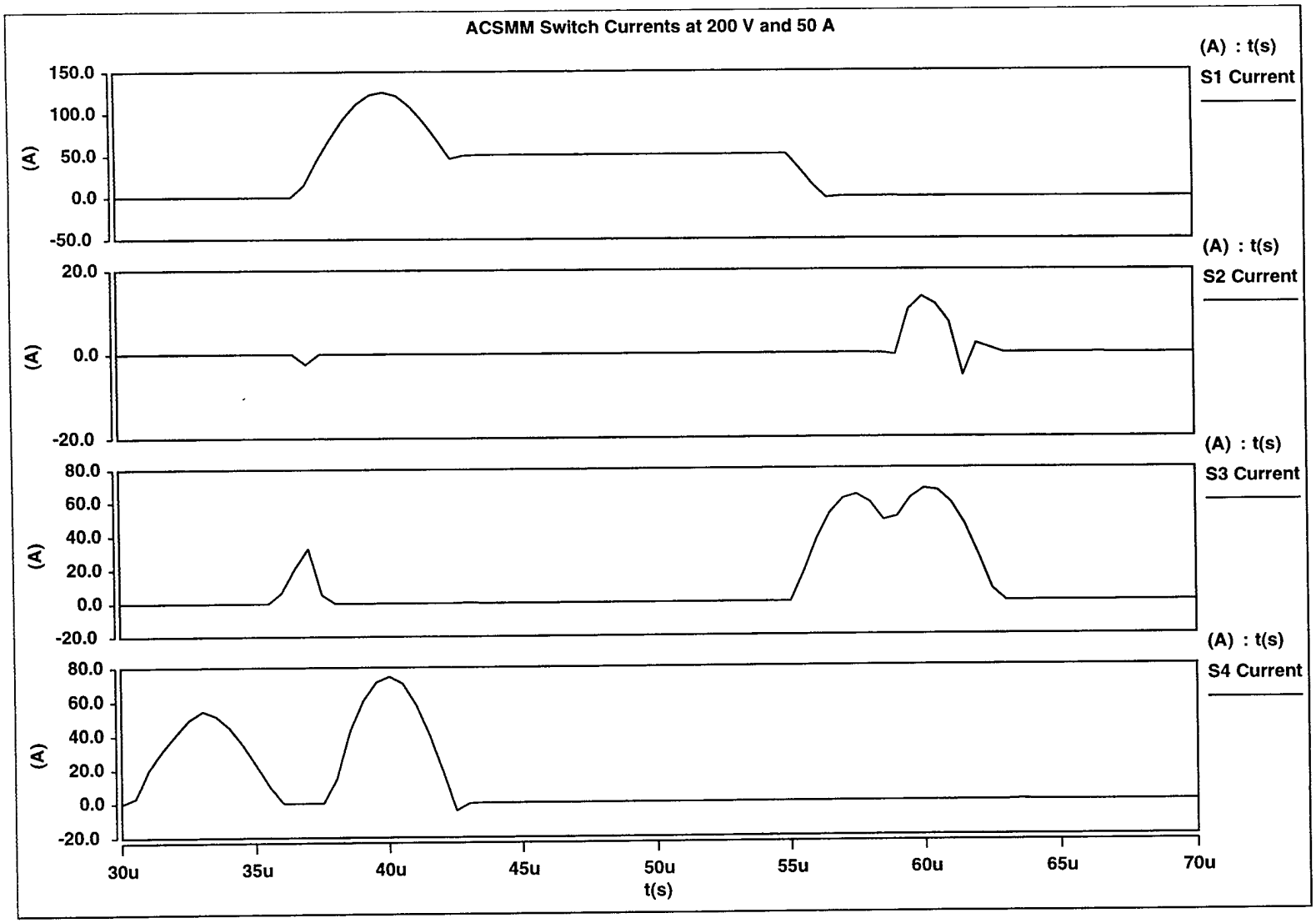

Figure 5.7 ACSMM Switch Currents

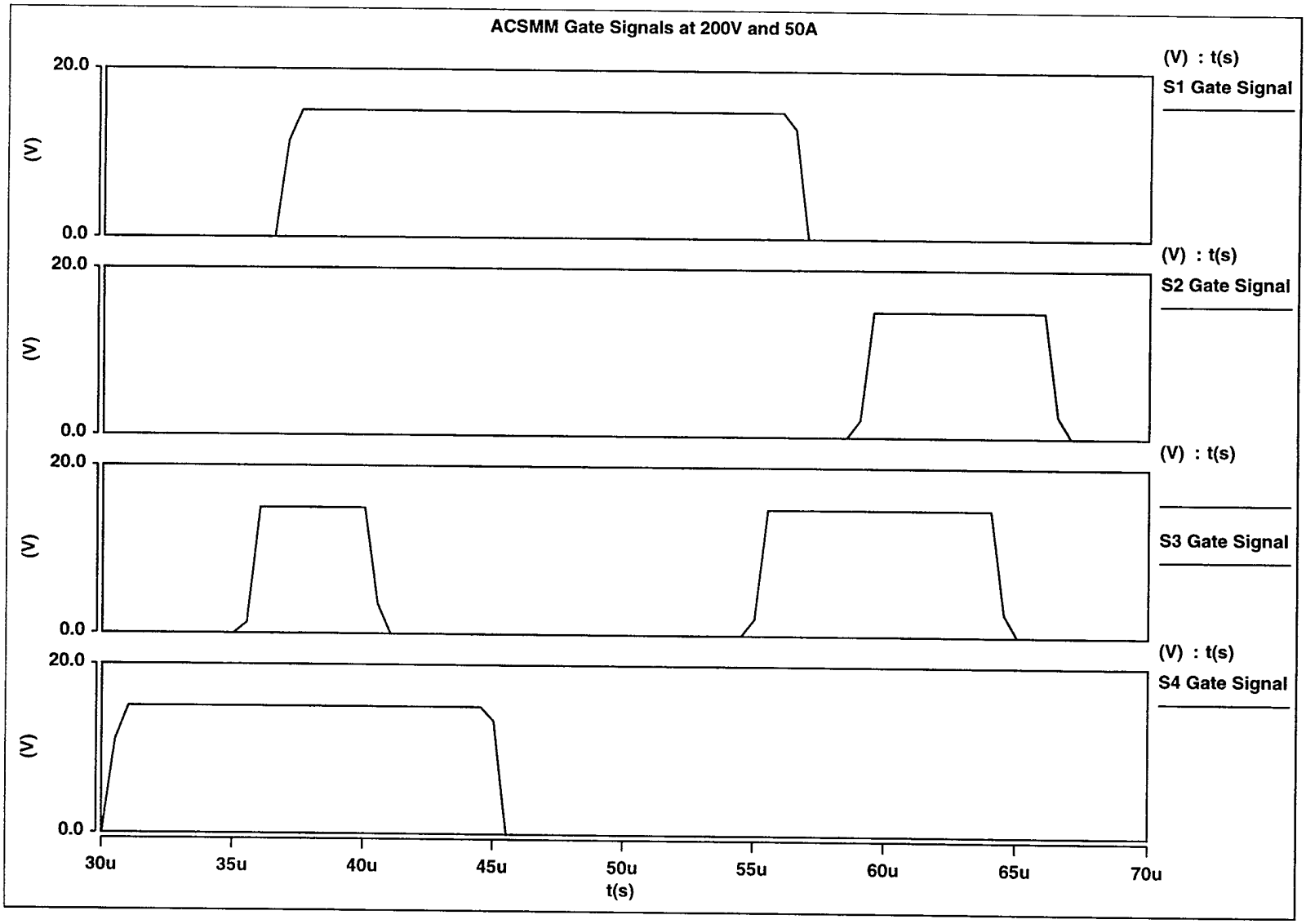

Figure 5.8 ACSMM Switch Timing

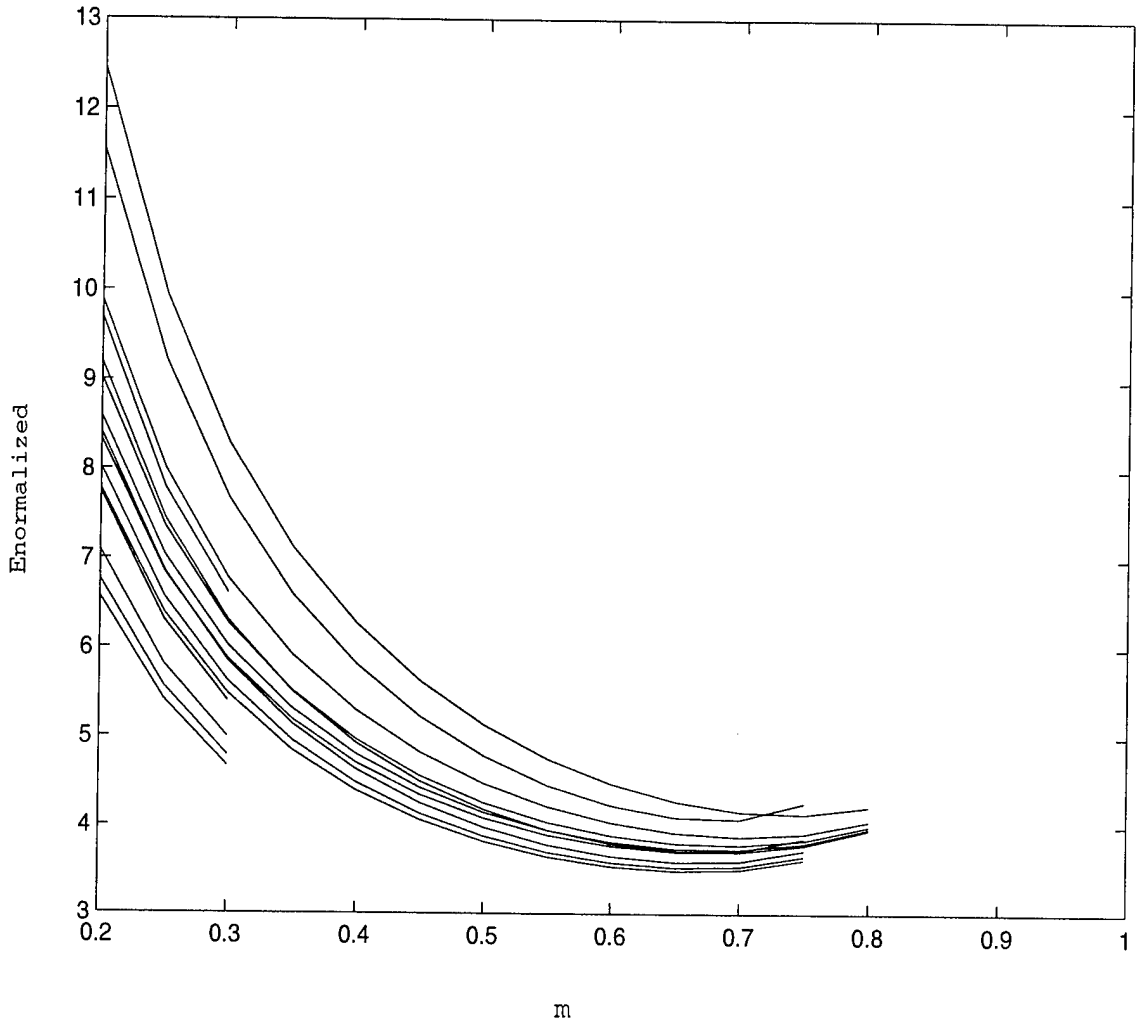

Fig. 5.9 Plot of Enorm vs. m

CHAPTER 6
CONCLUSION

Four zero-current switching topologies and associated switching strategies have been presented in this report. Each topology/strategy proved to have strengths and weaknesses. Some common weaknesses are the long turn-around time associated with multiple resonant cycles and uncertainties associated MCT performance, particularly the presence and/or duration of a circuit-commutated turn off time, t_q.

The long turn-around times are most prevalent in the MLZDCB (resonant bridge with zero-current turn-off and zero current turn-on) of Chapter 2 and the ACSMM (PEBB1 switch topology with zero-current turn-off and adjustable-current turn-on) of Chapter 5.

The BRDCY (resonant bridge with blocking diodes) presented in Chapter 3 appears to be require considerable thought and redesign due to a trapped energy problem, which was explained and demonstrated in analysis. Additionally, the diode recovery problems that were witnessed in simulations may not improve with more detailed simulations. Further investigation and possible hardware implementation are not recommended for this strategy.

The Resonant Bridge of Chapter 4 does show some promise. The primary limitation of this strategy is the recovery transient on the opposite diode during main switch turn-on. This turn-on under load is used to reduce the turn-around time, the primary reason for its design. If a diode that can withstand this type of reverse recovery transient can be obtained; this strategy would offer significant promise because of the significant improvement in turn-around time that it presents. More detailed simulations, concentrating on better diode models and implementations of the detailed MCT models are recommended for this strategy prior to any hardware implementation.

The primary question that remains to be answered is whether a zero-current switching topology will be superior to a zero-voltage topology such as the ARCP. Preliminary indications are that this may be the case. Further study to include detailed

simulations with MCT's and hardware implementations utilizing MCT's will answer this question. This task is not trivial due to the lack of MCT simulation models that must be developed and incorporated into designs. However, if the MCT proves to show significantly improved switching characteristics under a zero-current switching strategy, as is suspected, then the investigation will yield the optimal PEBB2 switching converter.

APPENDIX A
PRIMER ON STATE-PLANE ANALYSIS

A.1 INTRODUCTION

State-plane plots provide a convenient graphical method for constructing and analyzing the time response of resonant circuits. In particular, these time-parametric plots of resonant inductor current i_L versus resonant capacitor voltage v_C can be represented as a sequence of easy-to-draw circular trajectories. By scaling the characteristic sinusoidal response of a resonant circuit to fit within projections of the current-voltage trajectory inflection points, these circular trajectories can be "unwrapped" readily into voltage-time and current-time plots.

A.2 A BASIC RESONANT CIRCUIT AND ITS RESPONSE

A simple but useful form of the state-plane plot can be deduced by considering the response of a simple resonant circuit. A circuit that represents the salient features of all topologies considered in this project is shown in Fig. A.1; this circuit reflects the fact that the resonant components in these topologies are always in a loop with the dc input voltage source or their non-common terminals are shorted through one of the rails. The voltage source in Fig. A.1 actually represents a step function that results from changes in the connectivity of the circuit as the conduction state of the switches changes. The magnitude of the step function is the dc input voltage V_s, the opposite of the dc input voltage - V_s, or zero. Each of these cases can be seen by considering the basic resonant bridge shown in Fig. A.2, which is obtained by simplifying each switch-diode pair in Fig. 1.2 to a single bi-directional switch. The case of V in Fig. A.1 being equal to V_s in Fig. A.2 corresponds to S1 and S4 being on, while the $-V_s$ case corresponds to S2 and S3 being on. The zero case occurs for S1 and S3 on or S2 and S4 on. Because the two poles in the resonant bridge do not generally switch simultaneously, the step functions go only

between zero and V_s or between zero and $-V_s$; they do not go between V_s and $-V_s$. Referring again to the circuit of Fig. A.1, it is assumed that the inductor can have an initial current $i_L(0) = I_{L0}$ and that the capacitor can have an initial voltage $v_C(0) = V_{C0}$

The response of the circuit in Fig. A.1 can be established using several different techniques, including direct solution of a second-order differential equation, time-domain state-space analysis, and Laplace transforms. We will use Laplace transforms through application of s-domain equivalent circuits. That is, we will redraw the circuit in Fig. A.1 in the s-domain, showing explicitly the initial conditions as ideal sources. This is done in Fig. A.3. From this figure, the inductor-current response can be derived as

$$I_L(s)\left(sL+\frac{1}{sC}\right)=\frac{V}{s}+LI_{L0}-\frac{1}{s}V_{C0} \tag{A.2-1}$$

$$I_L(s)=\frac{I_{L0}s+\frac{1}{L}(V-V_{C0})}{s^2+\frac{1}{LC}} \tag{A.2-2}$$

$$I_L(s)=\frac{\frac{V}{s}+LI_{C0}-\frac{1}{s}V_{C0}}{sL+\frac{1}{sC}}\frac{\frac{s}{L}}{\frac{s}{L}} \tag{A.2-3}$$

$$I_L(s)=I_{C0}\frac{s}{s^2+\frac{1}{LC}}+\sqrt{\frac{C}{L}}(V-V_{C0})\frac{\frac{1}{\sqrt{LC}}}{s^2+\frac{1}{LC}} \tag{A.2-4}$$

$$i_L(t)=I_{C0}\cos(\omega t)+\sqrt{\frac{C}{L}}(V-V_{C0})\sin(\omega t) \tag{A.2-5}$$

The capacitor voltage response can be derived as

$$v_C(t) = \frac{1}{C}\int_0^t i_L(\zeta)d\zeta + V_{C0} \tag{A.2-6}$$

$$v_C(t) = \frac{1}{C}\int_0^t [\ I_{C0}\cos(\omega\zeta) + \sqrt{\frac{C}{L}}(V - V_{C0})\sin(w\zeta)\ ]d\zeta + V_{C0} \tag{A.2-7}$$

$$v_C(t) = \frac{1}{C}\left[\sqrt{LC}I_{C0}\sin(\omega t) - C(V - V_{C0})(\cos(\omega t) - 1)\right] + V_{C0} \tag{A.2-8}$$

$$v_C(t) = \frac{1}{C}\left[\frac{I_{C0}}{\omega}\sin(\omega\zeta) - \frac{\sqrt{\frac{C}{L}}(V - V_{C0})}{\omega}\cos\omega\zeta\right]\Bigg|_0^t + V_{C0} \tag{A.2-9}$$

$$v_C(t) = \sqrt{\frac{L}{C}}I_{C0}\sin(\omega t) - (V - V_{C0})\cos(\omega t) + V \tag{A.2-10}$$

A.3 STATE-PLANE PLOTS

To provide the most convenient form for plotting the circuit response, (5) and (10) can be normalized by multiplying by the square root of L and the square root of C, respectively. This yields

$$\sqrt{LI_{co}^{\ 2} + C(V - V_{co})^2} \tag{A.3-1}$$

From analytical geometry, a plot of the time-varying components of current vs. voltage is a circle. When the circle is centered at zero, the radius corresponds to the (constant) total energy in the resonant circuit. For convenience, the normalizing factors square root L and square root C will be dropped in subsequent discussions and are omitted throughout the body of this report. It should be understood that results obtained from the state-plane plot and corresponding voltage-time and current-time plots can always be scaled by these factors to determine the expected value of a quantity in the actual circuit.

In addition to knowing that the response of a resonant circuit follows a circular trajectory in the state-plane, it is also important to note that the nature of the capacitor

voltage and inductor current as state variables dictates that the trajectories be continuous. That is, if one were to follow the trajectory with a pencil, then he would never have to lift the pencil off the paper. A key implication of this is that the response of the entire switching circuit over a (PWM) switching cycle can be constructed from a sequence of intersecting circular trajectories. The center point of each successive trajectory is determined by the polarity of the dc-input voltage relative to the resonant component as determined by the conduction state of the switches in the corresponding interval. The radius of each trajectory is simply the distance from the center point to the point of intersection with the previous trajectory – this satisfies both the circular and continuity constraints.

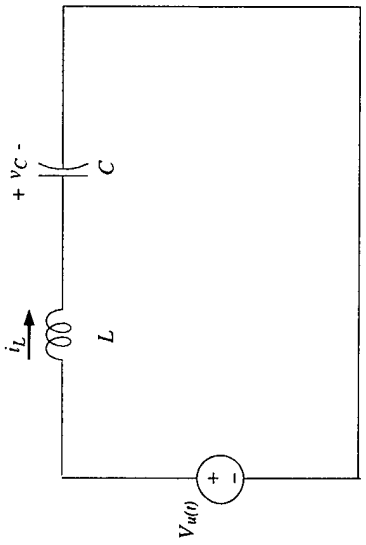

Figure A.1 Basic resonant circuit.

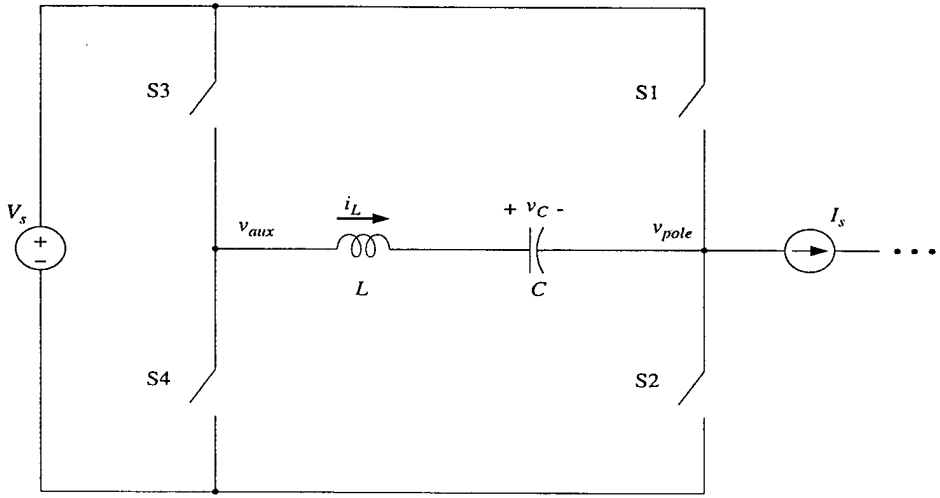

Figure A.2 Basic resonant bridge simplified to show each switch and its anti-parallel diode as a bidirectional switch.

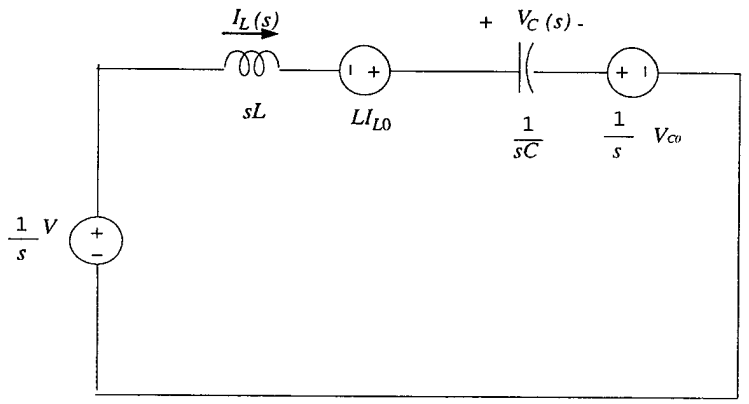

Figure A.3 s-domain simplified resonant circuit.

APPENDIX B
CURRENT SENSING METHODS

For several of the control methods described in this report it is necessary to have some information regarding the instantaneous value of the resonant inductor current i_L (or at least its zero-crossing time) be available to the DSP. There are several methods for sensing this current including:

1. LEM current sensor.
2. Sense resistor, differential amplifier, and isolation amplifier.
3. Sense resistor, differential amplifier, and instrumentation amplifier.
4. Sense resistor, differential amplifier, and optocoupler (only indicates zero-crossing).
5. Hardware integrator of inductor voltage.
6. Software integrator of inductor voltage.

Key features of each of the first four of these methods are described in this appendix.

B.1 LEM CURRENT SENSOR

A LEM sensor provides an extremely convenient and robust means for measuring power-frequency currents but is relatively expensive, and it is not obvious from data-sheet specifications that a LEM can be used to measure the relatively high-frequency resonant currents associated with the converters described in this report. Past experience, however, has shown that LEM specifications are often very conservative and have continually improved. To evaluate the suitability of present LEM sensors for use in prototype zero-current switching converters, the PSU/ARL ARCP was modified and run at 190 V and 36 A. A model LA-55-P LEM sensor was inserted with six turns on the auxiliary circuit inductor. The added inductance of the turns resulted in a resonant frequency of 200 kHz. The ARCP was operated at 50 kHz and current measurements were recorded using a pen plotter. While the ARCP is a zero-voltage switching converter, the auxiliary circuit inductor current in that converter is similar in form to that that of the BRDCY resonant inductor current.

A plot of a single pulse is shown in Fig. 1, which illustrates the gate commands of the main switches as Channel 2 and 3. The actual current as measured by a current probe (20 MHz bandwidth) is shown as Channel 4 and the current measured by the LEM sensor shown as Channel 1. There is considerable ripple in the LEM sensor output as the pulse current ends. This may be the noise that was noted by NSWC personnel during previous experiments. The total delay between the actual current and the detected current (via LEM) is on the order of 100ns.

For prototype converters on the order of 100 kW, the suggested part is the LA-125-P, which could accommodate peak resonant currents on the order of 250 A with *di/dt* rates of 200 A/μs. It is possible that the peak current could be pushed to over 400 A, based on the above tests, although this is not definite. The expected delay, based on discussions with LEM-USA is on the order of 200 ns or less. A schematic for a current sensor based on a LEM is shown in Fig. B.2. The main advantages of this method are the convenience provided by the LEM's inherent isolation and the availability to transmit full waveform information to the controller.

B.2 Isolation Amplifier

The schematic of a current sensor based on an isolation amplifier is shown in Fig. B.3. The primary advantage of this method is that full waveform information can be transmitted across the voltage boundary using a relatively small circuit. This method suffers, however, from a significant delay that is on the order of 1.2 to 1.3 μs (small signal bandwidth). Utilizing this method at a higher resonant frequency than 100 kHz would be difficult.

B.3 Instrumentation Amplifier

The schematic of a current sensor based on an instrumentation amplifier is shown in Fig. B.4. Use of an INA-117A instrumentation amplifier, will allow bandwidths approaching 200 kHz with response times on the order of 0.65 μs for detection of the zero current crossing. Here the disadvantage is that the controller will only be isolated by and impedance of 200 to 700 kΩ, depending on the isolation network chosen. While this will prevent power current from flowing in the controller ground, it will couple considerable high frequency noise into the controller. This method also requires the use

of high precision resistors, which are costly and generally have long lead times. The suggested source for these resistors, if this method is chosen, is RCD.

B.4 Current Threshold Sensor

For control strategies that require only zero-crossing information, the current threshold sensor shown in Fig. 5 can be used. Here the decision about the zero crossing is determined by a comparator, which then transmits the status of the current (i.e. higher than or less than zero or another threshold value) to the controller. The isolation is complete, the interface is simple, and the response time for the devices shown (including optocoupler) is on the order of 320 ns. This is based on the comparators response time of 180 ns, hysterisis loop of 20 ns, sense resistor rise time, with capacitor of 45 ns and optocoupler response time of 75 to 85 ns. The disadvantage of this approach is that the decision is made on the sampling side of the isolation boundary. This results in a significant loss of information to the controller, and the possible error introduced by needed hysteresis around the comparator.

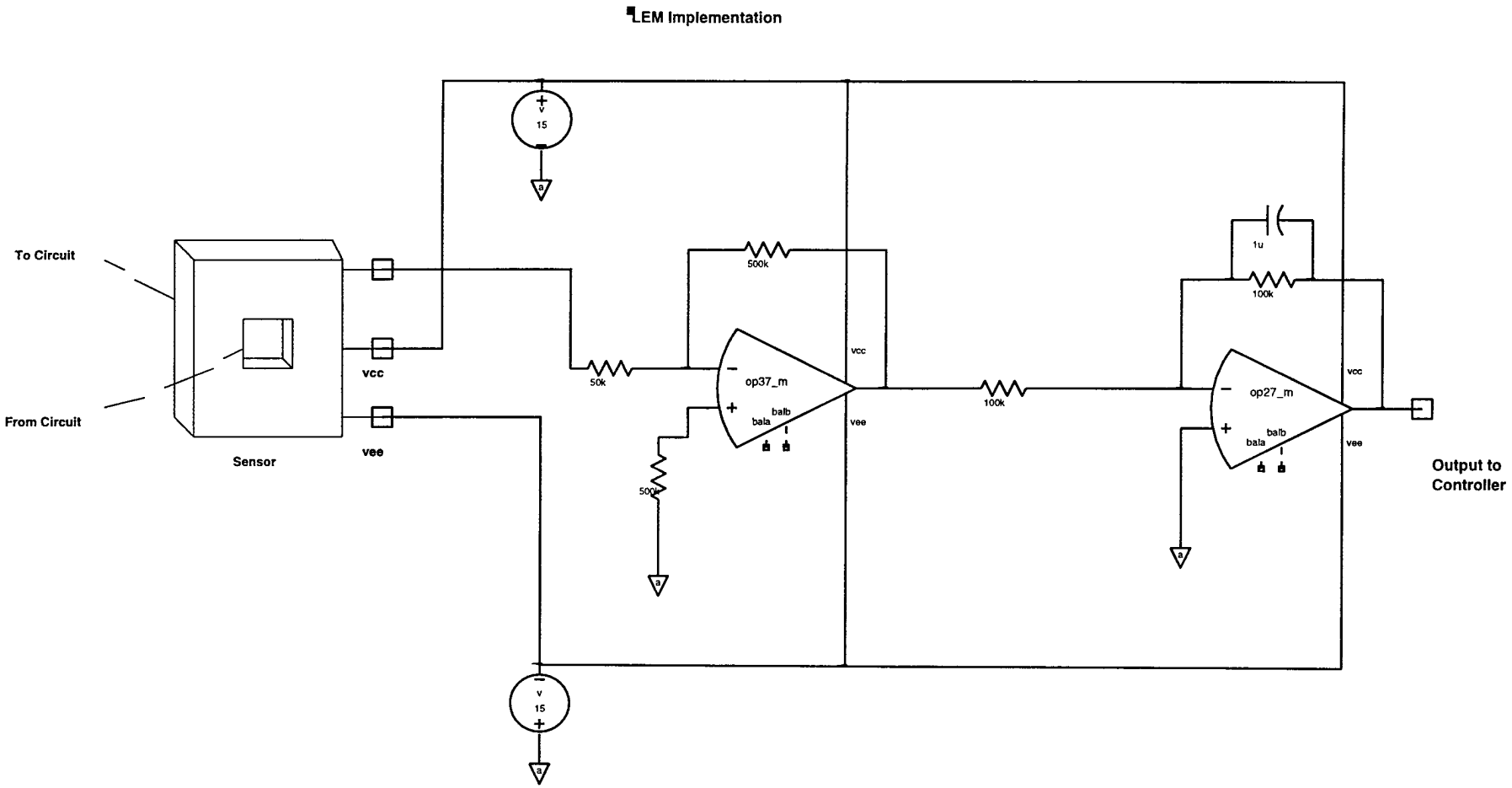

Figure B.2 LEM Sensor Implementation

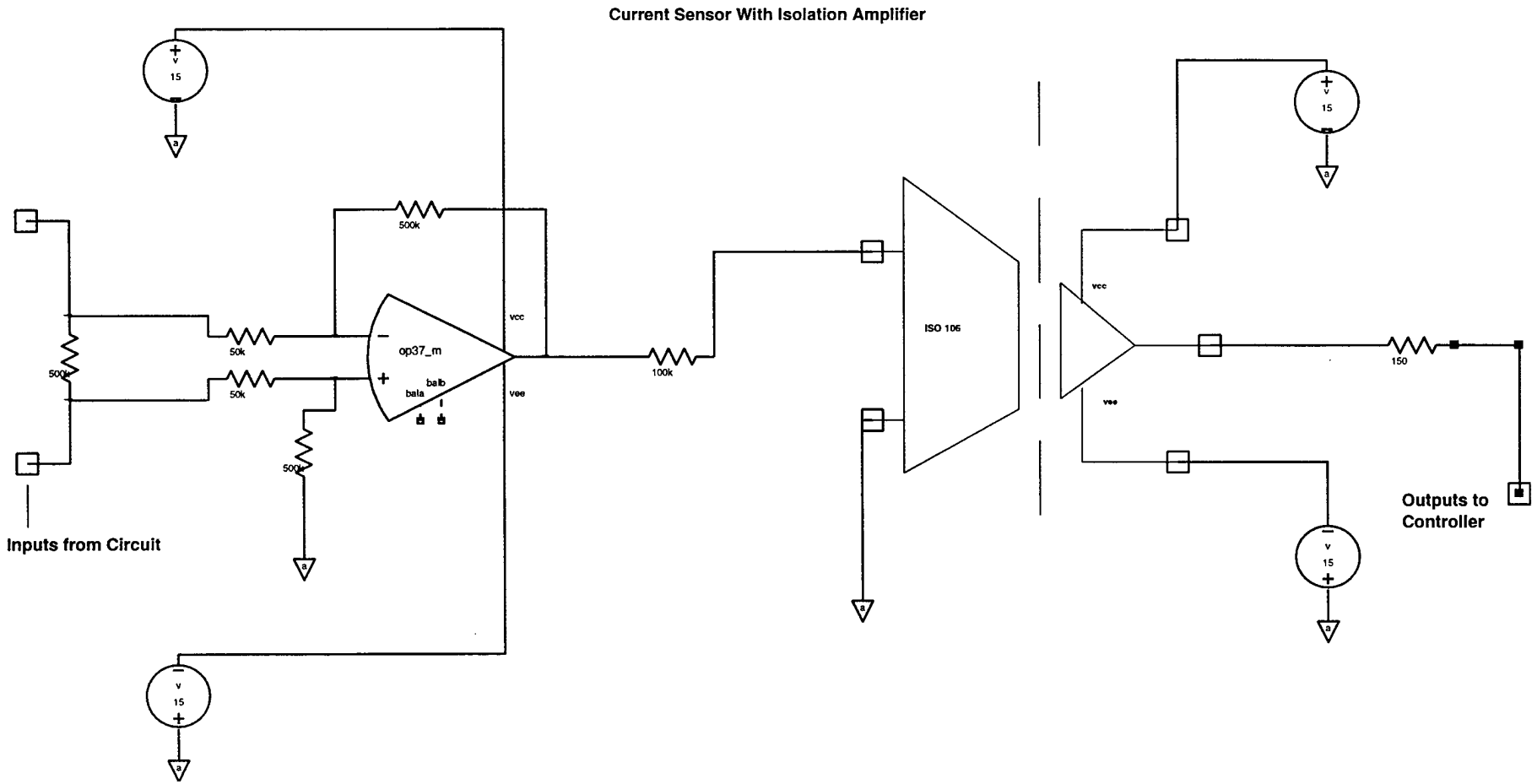

Figure B.3 Current Sensor with Isolation Amplifier

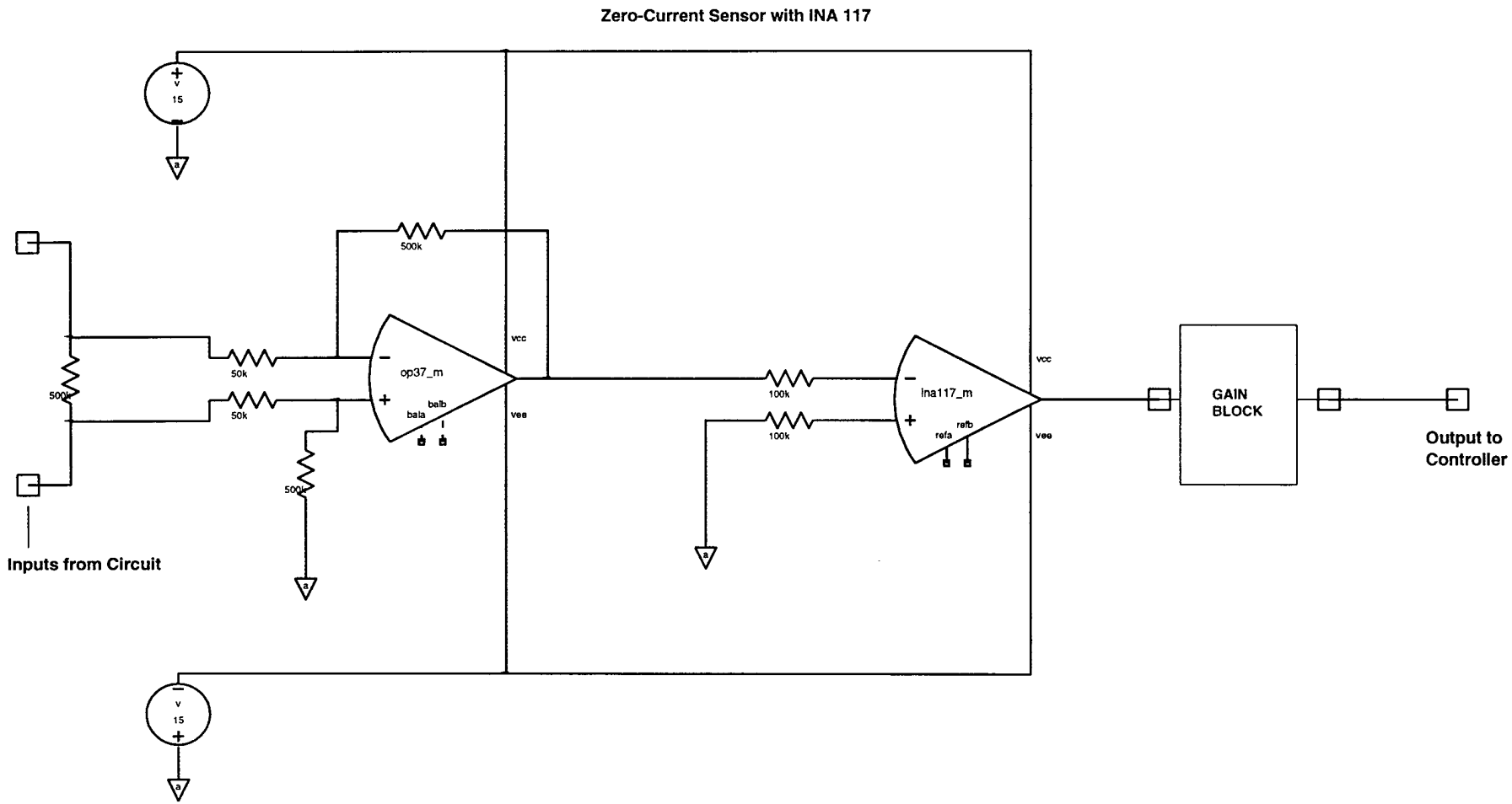

Figure B.4 Current Sensor with INA-117

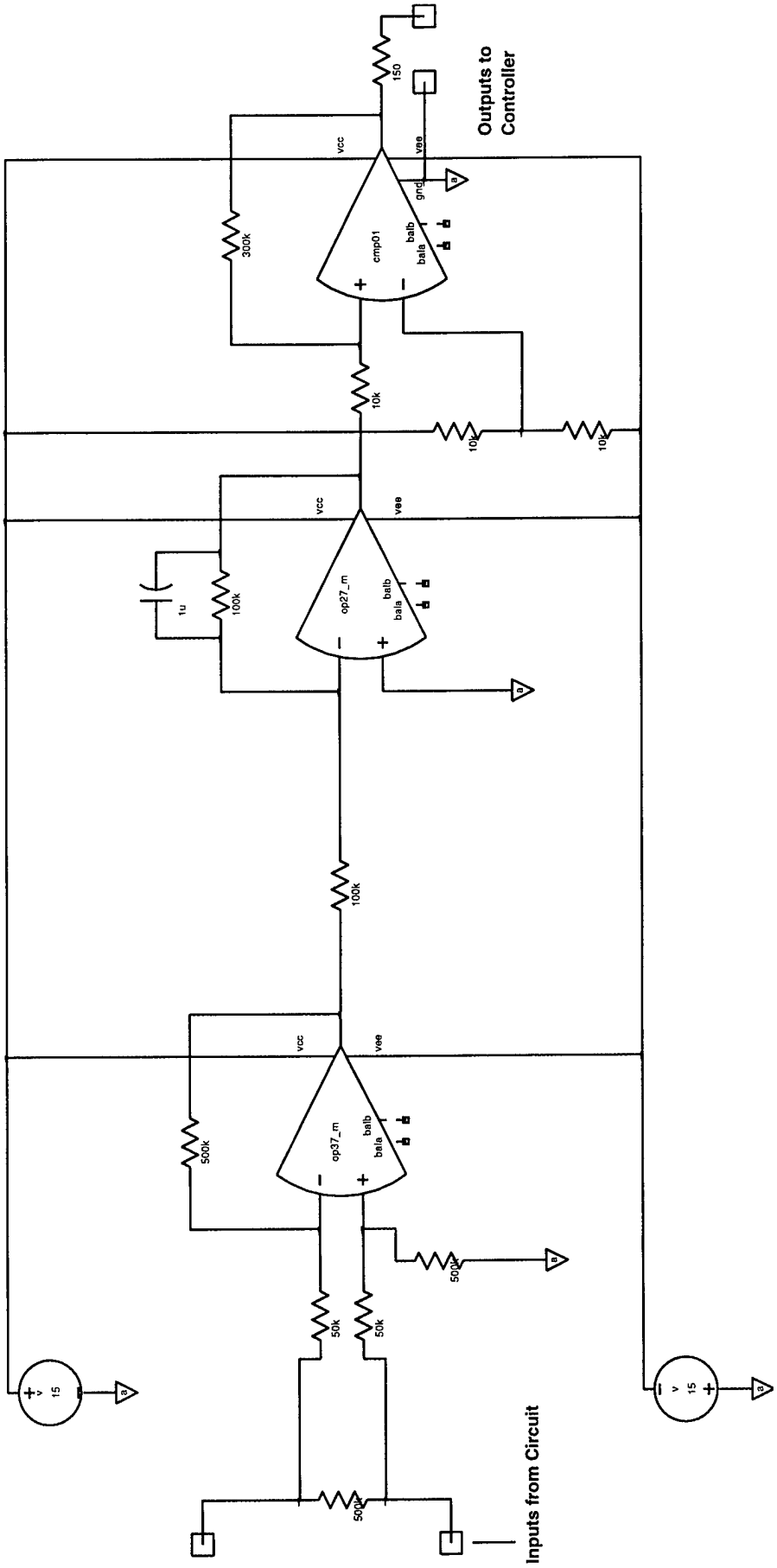

Figure B.5 Current Sensor

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